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Impact of SEG on uniaxially strained MuGFET performance

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ABSTRACT

This work focuses on the impact of the source and drain Selective Epitaxial Growth (SEG) on the performance of uniaxially strained MuGFETs. With the channel length reduction, the normalized transconductance (gm.L/W) of unstressed MuGFETs decreases due to the series resistance and short channel effects (SCE), while the presence of uniaxial strain improves the gm. The competition between the series resistance (R_s) and the uniaxial strain results in a normalized gm maximum point for a specific channel length. Since the SEG structure influences both R_s and the strain in the channel, this work studies from room down to low temperature how these effects influence the performance of the triple-gate FETs. For lower temperatures, the strain-induced mobility enhancement increases and leads to a shift in the maximum point towards shorter channel lengths for devices without SEG. This shift is not observed for devices with SEG where the strain level is much lower. At 150 K the gm behavior of short channel strained devices with SEG is similar to the non SEG ones due to the better gm temperature enhancement for devices without SEG caused by the strain. For lower temperatures SEG structure is not useful anymore.

1. Introduction

With the continuous scaling down of MOS devices and consequently the technology development, the short channel effects (SCE) become more important. Multiple gate devices (MuGFETs) on SOI wafers appear as an alternative due to their better channel charge control by the gates mainly for narrow devices. Triple-Gate FETs emerge as one of the best candidates to MOS transistors owing to the better SCE, the transconductance increase and almost ideal sub-threshold slope [1]. However, tri-gate FETs suffer from high parasitic source/drain series resistance that degrades the device performance. In order to reduce the source/drain series resistance (R_s), the Selective Epitaxial Growth (SEG) technique is frequently used [2,3].

In addition, mechanical stress has been used with the objective to boost the mobilities and consequently enhance the device performance. Recent studies reported a 60% increase in electron mobility when SOI MOSFET transistors are under tensile mechanical strain. Accordingly, the transistors present a higher transconductance and drain current without an increase in its leakage current [4]. Two different kinds of techniques have already been used in order to induce strain in the channel. The first one addresses the cases in which the whole wafer is strained at the same time (biaxial) and the second one is related to local strain application (uniaxial). Although the maximum achievable stress levels are lower, the second technique is considered to have better scaling properties [5–8].

At the same time, it is known that the SEG S/D structures, which are normally used to decrease R_s, can also degrade the strain efficiency. Therefore, this work discusses the relationship between the use of SEG and the uniaxial strain engineering on the transconductance behavior in triple-gate SOI transistors.

Considering that the low temperature operation improves the MOSFETs performance [9] and also increases the strain efficiency, both resulting in a higher mobility [10], the behavior of CESL plus SEG at low temperature is also studied.

2. Device characteristics

The studied triple-gate nFinFETs are fabricated on SOI wafers with the following characteristics: 150 nm buried oxide thickness, 65 nm top silicon layer thickness (H_{FIN}) and 2.3 nm HfSiON on 1 nm SiO_2 as gate dielectric. The midgap metal gate is obtained by deposition of a 5 nm TiN layer and a 100 nm thick polysilicon capping to complete the gate electrode. No channel doping is applied during the processing resulting in a natural wafer doping ($N_a = 1 \times 10^{15}$ cm^{-3}) [11]. The uniaxial tensile strain was induced

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by a 100 nm nitride contact etch stop layer (CESL). For both standard and uniaxial devices the channel width (W_{FIN}) was kept constant and equal to 20 nm and the analyses were performed for a channel length (L) ranging from 900 nm down to 30 nm. Devices with and without SEG were also evaluated for both cases (standard and uniaxial ones) and the SEG thickness (t_{SEG}) is 30 nm.

The measurements were performed as a function of temperature from 300 K down to 200 K. These characterizations were done using the Variable Temperature Micro Probe System model K20 from MMR Technologies and the experimental curves were extracted using an Agilent 4156C semiconductor parameter analyzer.

Process simulations were performed to better understand the mechanical stress distribution in the channel, induced by the tensile capping layer in devices with and without SEG. A schematic view of the device is shown in Fig. 1.

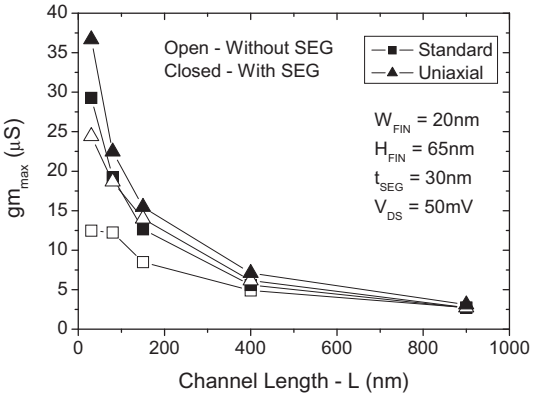

Fig. 2. Experimental gm_{max} behavior for standard and uniaxial strained devices, with and without SEG at room temperature.

3. Analysis and discussions

Fig. 2 presents the experimental maximum transconductance (gm_{max}) behavior as a function of the channel length for uniaxially strained devices and standard (unstrained) ones with and without SEG. It can be seen that for devices with SEG the maximum transconductance is higher than for devices without SEG due to the smaller parasitic source/drain series resistance (R_s). It occurs for both strained and standard transistors. This effect is more pronounced for shorter devices, where R_s is more important compared to the transistor channel resistance (R_{CH}). Comparing the strained and unstrained devices, one can observe that for longer devices the gm_{max} is almost the same because the uniaxial strain has no influence on longer devices. However, the strain efficiency increases as the channel length is reduced resulting in a higher drain current due to the mobility increase. The drain current increase results consequently in a higher gm_{max} point. If SEG is used on uniaxial strained devices at room temperature, gm_{max} is higher as shown in Fig. 2.

In order to eliminate the transconductance dependence on the device dimensions, the gm_{max} curves versus channel length were normalized by the L/W_{eff} ratio, where $W_{eff} = W_{FIN} + 2\ H_{FIN}$. Fig. 3 shows the normalized maximum transconductance behavior as a function of the channel length for standard and uniaxial devices, both with and without SEG at 200 K (Fig. 3A) and 300 K (Fig. 3B).

Taking into account that the transconductance dependence with channel length and channel width was removed with the gm normalization, the transconductance decrease can be attributed first to the series resistance and also to the SCE for shorter devices. For both standard and uniaxially strained devices, the presence of SEG results in a higher contact area at drain and source that reduces the series resistance, where the gm roll-off is smaller than for devices without SEG. However, when the focus is on the uniaxially strained devices an additional increase in the gm_{max} is obtained due to strain influence on the electron mobility. For devices with channel lengths smaller than 60 nm the gm roll-off is also caused by the SCE.

The same behavior was observed at room temperature and at 200 K, but at low temperature (200 K), the gm_{max} increase is observed due to the mobility improvement.

The presence of SEG, improves the gm due to the reduction of the series resistance and at the same time causes a reduction of the efficiency of mechanical stress induced by the capping layer,

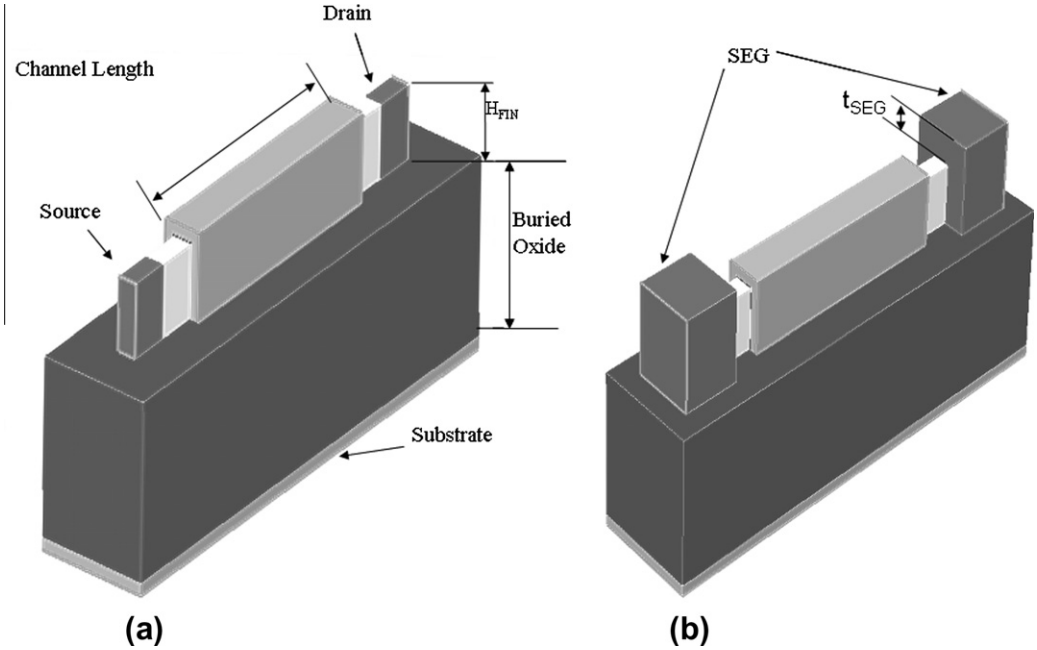

Fig. 1. Schematic representation of the studied Triple-Gate FETs without (a) and with (b) SEG.