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Improving the cell characteristics using arch-active profile in NAND flash memory having 60 nm design-rule

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ABSTRACT

Recently the cell integration density of NAND flash memory is increasing rapidly due to its simple structure, which is suitable for high resolution lithography. Therefore, the reduction of cell size has become the most important issue. However, with an increase in the number of cells and the downscale of cell size, the NAND cell string has problems of not only small on-cell current and poor program speed but also current fluctuation due to random telegraph signal (RTS) noise. In this paper, in order to overcome revealed problems, we would like to propose the floating gate NAND flash memory, which has an arch structure active region. Also, we applied the arch structure on a poly-Si/W_{six} stack gate of 60 nm design-rule NAND flash device for the first time, which improved cell operation characteristics such as cell current, program speed and current fluctuation ($\Delta I_d/I_d$) due to RTS noise.

1. Introduction

NAND flash memory is one of the nonvolatile memory devices which can hold programmed data without a power supply. Recently, with the wide spread of portable equipment in audio/video fields such as MP3 players and digital still cameras, the demand for low-cost and high-density flash memory has dramatically increased. These applications commonly need solid-state mass storage devices, which feature high density, low-cost, low power, nonvolatility, and portability. The NAND flash memory can easily satisfy the above needs. However, with an increase in the number of cells and the downscale of cell size, the NAND cell string has a smaller on-cell current. In fact, the NAND cell string generally produces a small on-cell current compared to a NOR flash cell because of the large channel resistance coming from the series connection of cells. The on-cell current of a NAND flash cell depends on the bias condition, the back pattern (the states of the unselected cell in the string), and the parasitic capacitance between the cells [1,2]. A best/worst case of the on-cell current is respectively measured on the erased cell with an erased/programmed back pattern. As the number of cells in a NAND string increase, the size of each cell decreases, which causes the reduction of the best/worst on-cell current. As the device size shrinks even more, not only the program speed decreases due to the smaller coupling ratio, but also the RTS noise, which is caused by the trapping and detrapping of a single carrier, becomes a serious concern [3–5]. In this paper, in order to increase the best/worst on-cell current and program speed, and to decrease the current fluctuation ($\Delta I_d/I_d$) by RTS noise, we propose the use of an active structure having the arch profile for improved cell characteristics by increasing the electric field at Si/SiO_2 surface due to the electric field concentration effect [6]. To our knowledge, we are the first to apply arch flash technology to a floating gate/W_{six} stack gate in 60 nm design-rule NAND flash memory. The best/worst on-cell current, program/erase speed, and current fluctuation due to RTS noise were measured and compared with those of conventional flash memory.

2. Fabrication of the arch cell

The process of an arch-active structure is shown in Fig. 1. After pad oxidation, SiN (CMP stopper layer) and a hard mask were formed, an active area was patterned by lithography and dry etch as shown in Fig. 1a. After the edge of the pad oxide was etched by HF solution, the arch-active profile was formed through radical oxidation as shown in Fig. 1b and c. As shown in Fig. 1d, shallow trench isolation (STI) was formed. The active structure having the arch profile could be observed from the scanning electron microscope (SEM) image as shown in Fig. 1d. Then, the trench

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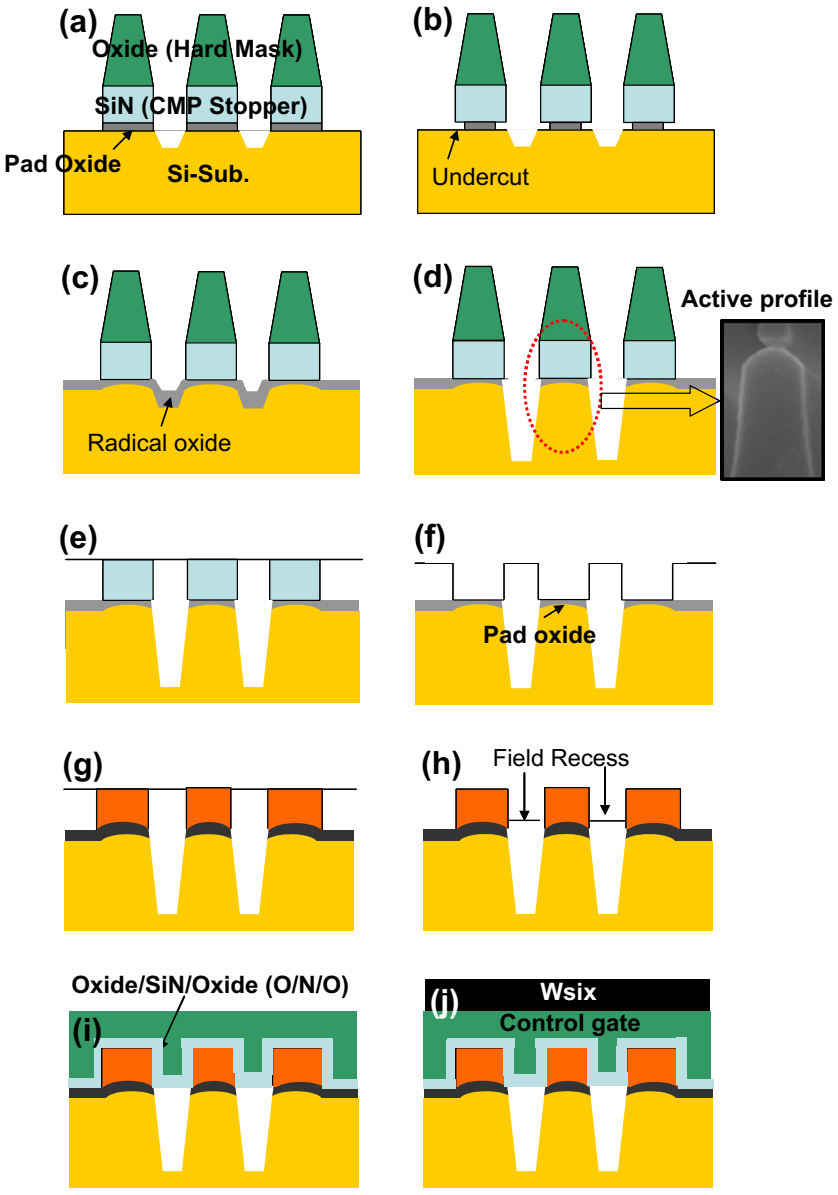

Fig. 1. Process flow of arch-flash memory. SEM image of (d) shows the active structure of arch cell after trench etch.

was filled by high density plasma (HDP) CVD oxide. Next, oxide chemical mechanical polishing (CMP) was conducted using the CMP stopper layer (SiN) as shown in Fig. 1e. After the wet etching of SiN and the pad oxide layer, tunnel oxide was then grown through radical oxidation in order to improve uniformity. Poly-silicon was then deposited for the floating gate. Finally, the floating gate was formed through the poly-silicon CMP process and field recess by using the wet etch process as shown in Fig. 1g and h. Oxide/SiN/oxide (ONO), poly-silicon (control gate) and W_{six} were then deposited in a row as shown in Fig. 1i and j. Fig. 2a and b shows the vertical structure for bit line direction (Y) and word line direction (X). The structure of a magnified arch cell can be clearly observed from the SEM image of the fabricated device as shown in Fig. 2c.

The cell current, program/erase speed and endurance characteristics were measured in a test of elements group (TEG) pattern having 32 cells array. Also, I_d fluctuation due to RTS noise was measured in the TEG pattern, which had a single cell, using the measurement equipment of RTS noise, which consists of a low noise amplifier (LNA), a dynamic signal analyzer (195 mHz to 102.4 kHz).

3. Results and discussion

There is almost no difference between the area of a planar and an arch cell because they have the same gate length (=65 nm) and active width (≈70 nm). Also, the tunnel oxide thickness of a planar cell is not different from that of an arch cell as shown in Fig. 3a and b. Since planar and arch cells have equal T_{ox} and area, their coupling ratio shows almost no difference. The electric field of a planar cell in the tunnel oxide is constant. However, the electric field of an arch cell is not constant due to the electric field concentration effect. Fig. 2c shows the vertical structure and model of an arch cell. Here, the electric field of the inner circle is defined by the following equation:

$$E(r_1) = E(r_2)\frac{r_2}{r_1} = E(r_2)\left(1 + \frac{T_{ox}}{r_1}\right) \quad (1)$$