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Impact of transparent conductive oxide on the admittance of thin film solar cells

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ABSTRACT

The impact of transparent electrically conducting oxide (TCO) on the admittance measurements of thin film p–i–n a-Si:H solar cells was investigated. Admittance measurements on solar cell devices, with different area and geometry, in a wide range of frequencies and biases were performed. The admittance measurements of the investigated solar cells, which use the TCO as an electrical contact, showed that the high frequency admittance per area unit depends on the area. This effect increases both with the probe frequency and the size of the solar cells. Transmission line model valid for strip geometry which explains how the resistivity of the TCO layer impacts the measured admittance of the p–i–n diode was presented. An estimate of the critical length of the strip solar cell over which the measured diode capacitance is affected by the TCO is given. The transmission line model allows to estimate also the lumped parasitic series resistance R_s of solar cells with strip geometry.

1. Introduction

Usually, thin film solar cells have transparent and conductive oxide film used as front contact of the p-type window layer. TCO may also be added at the bottom of the cell between the n-doped layer and the rear metal contact to increase back reflection. Metal grids are used at the front face to collect the distributed photo-generated carriers.

One of the most important requirement which these films have to meet is the low resistivity. Among the various TCO films, Al-doped ZnO (AZO) and F-doped SnO_2 are good candidates, especially in amorphous silicon solar cells. The effects of the TCO resistivity on the performances of solar cells are known and have been widely investigated [1–5]. The distributed series resistance of the TCO layer causes a detrimental effect on the efficiency of the cells, which increases by decreasing the thickness of the TCO layer and by increasing the area of the cells and the TCO resistivity.

The current work addresses the issue of the impact of the TCO on the admittance measurements and shows that the TCO resistivity also affects the admittance of p–i–n solar cells and that the impact of the TCO resistivity on the admittance is more pronounced as the frequency and the size of the cells increase. The measurement and the quantitative analysis of such effects may be used to monitor different TCO/metallization schemes of solar cells. Moreover, the frequency dependence of the admittance in a particular TCO/metal layout may have important effects on the data analysis of admittance spectroscopy measurements.

The admittance spectroscopy technique and the capacitance measurements are investigation tools used to characterize the performance and quality of solar cells which use different materials, such as a-Si:H [6] and polycrystalline $Cu(In,Ga)Se_2$ (CIGS) [7].

Usually, the admittance is measured on thin film solar cells which have TCO as front and back contact. In some cases the back contact is covered with metals such as Al or Ag. The instrument used to measure the admittance (usually an LCR meter) is connected to the solar cell under test with metal probes, which contact the TCO of the solar cells. For the analysis of the measured admittance, as far as we know, the TCO is treated as a metal and hence its resistivity is not included in the models (see, e.g. Refs. [6,7]).

We will illustrate that in solar cells the measured admittance is affected by the TCO layers. We have characterized thin films homojunction p–i–n a:Si-H solar cells with several areas and two different geometries, circular and strip. We have observed that the admittance per unit area depends on the size for the samples with large area, especially at high frequency. We demonstrate that this effect is due to the resistivity of the TCO layer, which is about two

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orders of magnitude higher than that of a metal, and occurs when the probe contact is small with respect to the area of the cell. We present a distributed model, based on the telegrapher's equation, valid for the cells with strip geometries, which confirms the experimental results. The analytical results allow to estimate the critical geometrical size of solar cells over which the capacitance measurements are sensitive to the TCO and its relation with the probe frequency and TCO resistivity, regardless of the material and the technology used to fabricate the solar cells.

Additionally, this model allows to predict the experimentally derived series resistance R_s of the solar cells with strip geometry.

2. Materials

The investigated a-Si:H p–i–n thin film cells were deposited at ST-Microelectronics (Catania, Italy) by plasma-enhanced chemical vapor deposition (PECVD) of SiH_4 at low temperature on SnO_2 substrate by AGC ASAHI GLASS. The thickness of the intrinsic layer is 250 nm and that of the doped layers are 20 nm. The back contact is obtained from the ZnO:Al deposition, 900 nm thickness, on the n-layer. These structures were fabricated as above described with only TCO contacts without additional metallization and realized on a 6" glass substrates. The cell contacts are made of TCO with no additional metal bus, thus the finite TCO resistivity can produce a significant series resistance which impacts the photovoltaic cells performances. The geometries are circles, with the following diameters 0.01, 0.02, 0.04, 0.08, 0.16, 0.32 and 0.64 cm, and strips of width 100 μm and length 0.01, 0.02, 0.04, 0.08, 0.16, 0.32 and 0.64, 1.30, 2.62, 5.26 and 10.5 cm.

3. Measurements

3.1. DC characterization

The solar cells were first analyzed by measuring the current density versus voltage (*J–V*) curves both in dark condition and with a sun simulator under standard conditions (AM1.5G 100 mW/cm^2). The *J–V* curves in dark are well approximated by the one-diode model, with ideality factor $\eta \approx 2$, up to forward bias ≈0.7 V. At higher bias voltages the ideality factor increases. The *J–V* curves under illumination of the solar cells show that the increasing of the area causes the deterioration of cell performances, due mainly to the decreasing of the short circuit current density (J_{sc}) and the fill factor (*FF*). The V_{oc} is almost constant with the cell area. From the measured *J–V* curves in dark we derived the series resistances of the samples by using two methods [8]: the first is a static method which deduces the series resistance from the gap between the actual curves $ln(I)$ versus V and the ideal diode curve with $\eta = 2$, the second is a dynamic method which obtain the series resistance from the intercept of the differential resistance dV/dI versus $1/I$. In both methods the effects of the shunt resistance are neglected.

3.2. Admittance measurements

The admittance measurements were performed using an Agilent 4980A LCR meter at voltage bias varying from −1.0 up to +1.0 V, with 30 mV ac oscillator amplitude. All measurements were taken in dark and at room temperature. We contact the top TCO AZO layer with the high terminal of the LCR meter, whereas the bottom TCO SnO_2 layer is held at the virtual ground by the low terminal of the LCR meter. The guard terminals of the probes are connected together in order to reduce the outcome of stray capacitance present between the measurement terminals and the closely located conductor of the chuck. The accuracy of the LCR depends mainly on the value of the measured admittance. Moreover, the accuracy of the measured capacitance is different from that of the conductance. Thus, to obtain an accuracy lower than a few % (of reading value), the frequency range of the measured capacitance is 100 Hz–2 MHz. At high frequencies the losses are large (quality factor $Q \to 1$) and the accuracy of the capacitance decreases. At low-frequency Q increases ($Q \gg 1$), so the accuracy of the measured conductance worsens (can be estimated Q times that of the capacitance). Hence, the lowest frequency of conductance measurements is 30 kHz for the devices with the smallest area.

We measured the capacitance and the conductance of the investigated solar cells at several frequencies and biases. The measured *C–V* and the *G–V* curves show the same behavior for both geometries.

At forward bias >+0.4 V both the measured capacitance and conductance at fixed frequency increase with the voltage bias. The low-frequency conductance is close to the differential conductance extracted from the *I–V* curves. The measured capacitance is the diffusion capacitance, which is mainly due to both trapped and free carriers in the intrinsic layer.

At reverse bias and up to +0.4 V the values of capacitance of the investigated cells are almost constant with both the bias and the frequency. The measured value is ≈50 nF/cm^2. In this range of the voltage bias the measured capacitance is the geometric capacitance $C_{geo} = \frac{\epsilon}{d}$ [7], where ϵ is the semiconductor's dielectric constant and d is the thickness of the intrinsic a-Si:H layer. The contribution of space charge and bulk traps to the capacitance of the p–i and n–i junctions cannot be detected at the used temperature and frequency range [6].

Fig. 1a shows the measured capacitance in reverse as a function of the frequency of the solar cells with circular geometry and with different areas. We note the cut-off of the capacitance at high frequencies only for the cells with the largest area.

In reverse bias and up to +0.4 V the values of conductance of the investigated cells are almost constant with the bias and increase with the frequency. Fig. 1b shows the conductance in reverse at −0.5 V normalized by angular frequency G/ω versus frequency of the solar cells with circular geometry and with different areas.

Generally, the analysis of the conductance curves can detect defect levels in the band gap, responsible to the losses. Each peak in G/ω is associated with a trapping level or a band with a characteristic time related to the peak frequency as ω_{peak}^{-1}. We note that the curves of the small area samples almost overlap and do not show any peak. Thus, losses associated with characteristic times are not observed in these devices. For medium diameters the curves increase over those of small area and for larger devices G/ω have a peak at a frequency value which decreases by increasing the area. These peaks correspond to the cut-off of the capacitance with the frequency. We will show that the peak in the normalized conductance and the cut-off in the capacitance for large area cells are not generated by defects present in the device, but is a circuital effect of the TCO impedance, which manifests itself only for the solar cells with large area.

In summary, the main feature of the admittance per unit area measured in reverse of the investigated cells is its dependence on the area itself, especially for large area devices and at high frequencies. For example, the peak in the G/ω curves present in large solar cell samples is not observed in small area samples.

The effect of the TCO on the measured capacitance of the p–i–n solar cells is more evident in Fig. 2, where the capacitance per area unit measured at the reverse bias −0.5 V and at 10 kHz, 100 KHz and 1 MHz is shown for the strip devices as a function of the length. We note that the capacitance is almost constant for low values of the length. Each curve shows a critical length L_c over which a decrease of capacitance occurs. The larger is the frequency the lower is L_c.