Solid-State Electronics 54 (2010) 1343–1348

Contents lists available at ScienceDirect

Solid-State Electronics

journal homepage: www.elsevier.com/locate/sse

Crystallographic orientation effects on the performance of InP-based heterojunction bipolar transistors

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ARTICLE INFO

Article history:
Received 11 January 2010
Received in revised form 19 April 2010
Accepted 21 April 2010
Available online 15 May 2010
The review of this paper was arranged by Prof. E. Calleja

Keywords:
InP
Heterojunction bipolar transistor
Orientation
Passivation

ABSTRACT

We report the crystallographic orientation effects in InP-based heterojunction bipolar transistors (HBTs). The DC and RF characteristics of DHBTs fabricated on the same wafer were found to be dependent on the emitter orientation. Self-aligned InP/InGaAs DHBTs with [0 1 −1] emitter direction exhibit higher current gains, more stable and also better RF performance, while maintaining similar breakdown voltages, as compared to [0 1 1] oriented devices. Most of the differences are attributed to the resulting emitter–base sidewall profiles obtained after mesa etching. Without ruling out piezoelectric and stress effects, generally observed in III–V based HBTs, a contribution to the orientation effect, especially on the DC characteristics seem to be related to the more effective extrinsic base passivation for the [0 1 −1] orientation. For a given bias point, the maximum oscillation frequency ($f_{\max}$) is also slightly higher in [0 1 −1] oriented devices, due to a smaller base resistance resulting from a smaller base–emitter spacing, while the cut-off frequency (f_T) remains comparable in both orientations.

1. Introduction

In recent years, heterojunction bipolar transistors (HBTs) have shown great potential for analog, digital, and mixed-signal applications requiring high-speed and high voltage swing [1,2]. Owing to their material and transport properties, InP-based DHBTs with cut-off frequencies in excess of 600 GHz have already been demonstrated [3–5]. Such a high-frequency performance requires, however, aggressively scaled devices with self-aligned base–emitter structures to reduce the extrinsic base resistance and the base–collector junction capacitance.

In practice, when the emitter–base junction area is reduced, the current gain degrades, however, significantly due to the surface recombination at the emitter periphery. This is referred to the so-called emitter-size effect. Surface effects have been a dominant source of gain degradation in III–V based HBTs and have been studied extensively [6,7]. The surface is a dominant recombination source in most common designs due to a high rate of recombination through surface states and to Fermi-level pinning at the surface [8]. Various techniques including the use of surface chemical passivation or the use of a wide-gap material, as a ledge, at the surface of the extrinsic base (surface between emitter mesa and base contact) [9,10] can reduce to a certain extent the surface recombination.

On the other hand, accurate models and optimization of the device physical effects (material structure and composition, crystallographic orientation, etc.) are also critical for the successful design of HBT-based circuits. For instance, the current gain of GaAs-based HBTs were reported to be strongly dependent on the emitter direction. In Ref. [11], AlGaAs/GaAs HBTs were found to have higher current gain for [0 1 1] emitter orientation (perpendicular to primary flat, PF) and lower in the [0 1 −1] orientation (parallel to PF). Based on previous studies on piezoelectric effects in FET-based devices [12,13], it was proposed that emitter stress created piezoelectric charges at the HBT's emitter–base interface and associated electric fields can enhance or inhibit surface recombination.

Later on, Baca et al. [14] found that InGaP/GaAs HBT current gain orientation dependence was qualitatively similar to that of AlGaAs/GaAs HBTs. The magnitude of the piezoelectric orientation effect has also been established to be dependent on other factors, such as process induced damage during dielectric passivation. In addition, a slightly higher cut-off frequency has been observed in [0 1 1] oriented non self-aligned devices.

In comparison to previous studies, Borgarino et al. [15] found that it is rather the [0 1 −1] orientation that results in better DC and low-frequency noise characteristics. This has been attributed to the surface recombination at the extrinsic base region and to the piezoelectric properties of III–V based semiconductor materials.

So far, very little has been discussed for InP-based HBTs [16–20]. Among few available data is the observed degradation of the

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doi:10.1016/j.sse.2010.04.008

base–emitter junction in InP/InGaAs HBTs under bias and temperature stress [16], which also strongly depended on the crystallographic orientation of the emitter mesa. In contrast to most results on GaAs-based HBTs, the degradation was, in this case, mostly worse for the devices perpendicular to the major flat [0 1 1].

Therefore, further studies on the orientation effects on III–V based HBTs, especially InP-based HBTs are required to identify and clarify the possible origins and degradation mechanisms due to orientation effects. The purpose of the present work intends to systematically investigate the orientation effects on the DC and RF device performance of InGaAs/InP DHBTs passivated with benzocyclobutene (BCB). The use of BCB alleviates piezoelectric and stress effects reported, so far, in SiN or SiO_2 passivated devices using various chemical vapour deposition (CVD) based techniques [14]. In addition to most studies of the orientation effects in III–V HBTs, which have mostly focused on the Gummel characteristics and the current gain, we also investigate any changes in the other characteristics such as the output characteristics, the diodes, and the RF performance.

As expected, we found that the current gain of self-aligned InP/InGaAs DHBTs has a strong dependency on the emitter direction. In agreement with the results of Kurishima et al. [16], DHBTs with [0 1 −1] emitter direction show higher current gains and more stable characteristics. In effect, the [0 1 −1] orientation results in a partial ledge passivation of the extrinsic base (due to positively sloped emitter sidewalls). Moreover, the breakdown voltage is relatively comparable for both orientations. Furthermore, both orientations exhibit a comparable cut-off frequency (f_T) when measured at a fixed bias point, while the maximum oscillation frequency (f_{max}) is slightly higher for [0 1 −1] oriented DHBTs. The variation of the cut-off frequencies as a function of the collector current shows better RF performance for the [0 1 −1] oriented devices, as compared to [0 1 1] oriented DHBTs, due to a degradation of the gain with bias in latter devices.

2. Technology

The InP DHBT layer structure was grown on 3″ semi-insulating InP substrates, in a multiwafer molecular beam epitaxy (MBE) system. The structure features a 20 nm highly doped compositionally graded InGaAs emitter cap layer followed by an InP emitter (40 nm, $6 \times 10^{17}\,cm^{-3}$), a (30 nm, $5 \times 10^{19}\,cm^{-3}$) graded InGaAs base, and a compositionally step-graded InGaAs/InGaAsP/InP collector (160 nm, $2 \times 10^{16}\,cm^{-3}$), to minimize collector current blocking effects. Carbon tetrabromide and solid silicon were used for p- and n-type doping, respectively.

The fabrication process relies on standard manufacturing techniques, including *i*-line stepper lithography and selective dry/wet etching. The growth details and a detailed description of the device technology have been reported elsewhere [21,22]. Briefly, the emitter was contacted with WSi, which served as a self-aligned mask for a selective dry/wet etch of the emitter. The InGaAs layers were etched with a phosphoric/peroxide-based solution. The InP was subsequently etched with a phosphoric/hydrochloric-based acid. The self-aligned emitter and base were contacted using non-alloyed ohmic contacts of Ti/Pt/Au and Pt/Ti/Pt/Au, respectively.

The emitter–base self-alignment is achieved by WSi selective dry etching, with an undercut of less than 200 nm in both directions. As will be discussed in the following section, the resulting emitter mesa to base metal effective spacing (d_{EB}) is critical for the device performance. After the base electrode formation, the process is completed with conventional processes and BCB for device passivation and planarization. Fig. 1 shows a top view SEM (scanning electron microscopy) photograph of a nominal $8 \times 1\,\mu m^2$ DHBT.

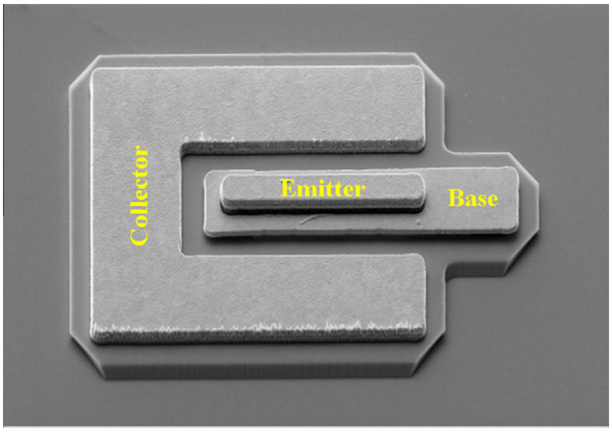

Fig. 1. SEM-picture of an InP-HBT with an emitter area of $8 \times 1\,\mu m^2$.

In this work, we compare two different emitter electrode orientations (Fig. 2): one emitter is oriented in the [0 1 −1] direction (parallel to the primary flat, PF) and the other is oriented in the standard [0 1 1] direction (perpendicular to PF). It is well known that wet etching of III–V based structures usually lead to anisotropic etching profiles according to the crystal orientations. As shown in Fig. 3, FIB/SEM (focused ion beam/scanning electron microscopy) cross sections reveal different emitter and base mesa profiles. The [0 1 −1] oriented DHBTs exhibit crystallographic (111) planes, which are at angles ∼55° with respect to the (0 0 1) plane. The positively sloped emitter mesa covers a large portion of the extrinsic base (Fig. 3a). The remaining exposed extrinsic base amounts to about 100 nm.

Similarly, this orientation also results in an outward sloped base mesa. The double stepped base mesa is due to the different etched materials (InGaAs/InGaAsP and InP).

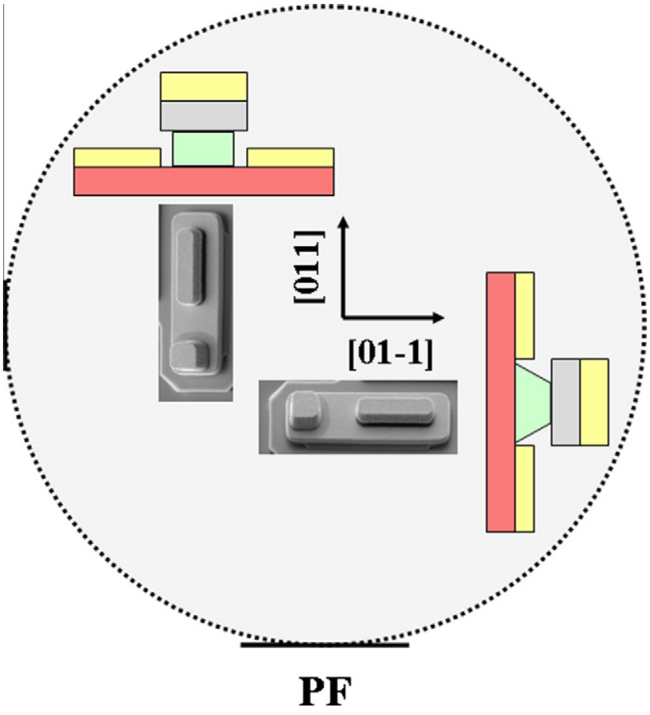

Fig. 2. Crystallographic orientation of the emitter mesa and self-aligned emitter–base contacts.