Solid-State Electronics 54 (2010) 1349–1358

Contents lists available at ScienceDirect

Solid-State Electronics

journal homepage: www.elsevier.com/locate/sse

Scaling projections for Sb-based p-channel FETs

M.G. Ancona *, B.R. Bennett, J.B. Boos

Electronics Science and Technology Division, Naval Research Laboratory, Washington, DC, USA

ARTICLE INFO

Article history:
Received 20 January 2010
Received in revised form 19 June 2010
Accepted 24 June 2010
Available online 23 July 2010
The review of this paper was arranged by Prof. S. Cristoloveanu

Keywords:
Hole transport
Antimonides
p-Channel
Device scaling
Density-gradient theory
Complementary circuits

ABSTRACT

Numerical device modeling is used to study p-channel FETs with InSb, GaSb and InGaSb channels. To be as realistic as possible, the basic parameters are chosen to be those measured experimentally in state-of-the-art high-mobility materials, and where possible, predictions are compared against published data. Confinement effects are captured in the simulations using the density-gradient description of quantum transport. The emphasis is on projecting scaling properties and ultimate performance, with key issues being short-channel effects, the importance of source-drain leakage current, power considerations and p^+-cap design. Although important, issues related to gate leakage current and gate stack design are not well addressed by modeling, and so are not considered in detail. With III–V complementary circuits and high-speed, low-power applications in mind, the general conclusion is that among the antimonide-based pFETs, InGaSb devices provide the best balance of speed and power dissipation.

Published by Elsevier Ltd.

1. Introduction

As a method for minimizing standby power, the CMOS approach of mainstream digital silicon electronics that employs matched n-channel and p-channel transistors provides a near-ideal solution. Of course one of the prime advantages of silicon is the facility with which it can implement complementary circuits, readily allowing the requisite enhancement-mode n- and p-channel transistors to be integrated in the same channel material, and with an easily grown, high-quality insulator in SiO_2. And this has been a major reason why silicon has dominated semiconductor electronics for many years. Recently, however, the quest for ever-better performance as envisioned by the ITRS roadmap has had researchers looking into the possibilities of CMOS circuits that utilize III–V materials, either alone or in hybrid form with germanium [1]. The main advantage of these alternative materials is their potential for higher speed at low voltage. Of course the III–Vs lack silicon's "natural fit" with CMOS – some of the main problems are the complications of heterogeneous materials integration, the lack of a good gate insulator, the generally lower material quality, the difficulties of achieving enhancement-mode, and the characteristically low values of the hole mobility in the III–Vs compared with their electron mobilities (see Table 1) – but recently significant advances have been made and the notion of III–V complementary circuitry is becoming more plausible [1]. A primary area of progress has been in III–V hole mobility, and the purpose of the present paper is to explore the scaling potential of these new pFETs, and to compare the relative performance of several candidate III–V materials.

Regularly achievable electron mobilities in the channels of III–V HEMTs at room temperature are much higher than in Si or Ge, e.g., in InAs they are in the range of 20–30,000 cm^2/V sec [2]. Such numbers have made the III–V semiconductors very attractive for fabricating high-speed n-channel transistors for use in analog circuits. In addition, the trend toward higher mobility with smaller bandgap (see Table 1) has made the III–V materials a route to achieving higher speed at lower voltage and on-state power for a given geometry as illustrated in Fig. 1 [3]. By contrast, the relatively poor hole transport properties and material quality of the III–V semiconductors has in the past yielded experimental p-channel mobilities that were limited to the range 100–300 cm^2/V sec [4]. The last few years have, however, brought encouraging progress. The starting point for these advances has been a focus on the antimonides that along with Ge have the most intrinsic promise as seen from Table 1. Pushing the hole mobilities even higher has then come via three strategies: (i) improving material quality, (ii) imposing strong confinement, and (iii) employing high levels of strain. The better quality materials are largely the products of long-standing programs on antimonide growth by molecular beam epitaxy at the QinetiQ Corp. (for InSb) and at the Naval Research Laboratory (for GaSb and InGaSb). When confinement and strain act on such materials, the hole mobilities are enhanced because, as in Si and SiGe [5], the degeneracy of the light- and heavy-hole bands is split, thereby raising the proportion of carriers in the

* Corresponding author.
E-mail address: ancona@estd.nrl.navy.mil (M.G. Ancona).

0038-1101/$ - see front matter Published by Elsevier Ltd.
doi:10.1016/j.sse.2010.06.022

Table 1
Bulk coefficients of various semiconductors at room temperature. Source: *Handbook Series on Semiconductor Parameters*, vol. 1, eds. M. Levinshtein, S. Rumyantsev, M. Shur, (World Sci., Singapore, 1996).

Semiconductor	Bulk electron mobility (cm^2/V sec)	Bulk hole mobility (cm^2/V sec)	Band gap (eV)
Si	1400	450	1.12
Ge	3900	1900	0.66
GaP	250	150	2.24
GaAs	8500	400	1.43
GaSb	3000	1000	0.67
InP	5400	200	1.29
InAs	40,000	500	0.33
InSb	77,000	850	0.16

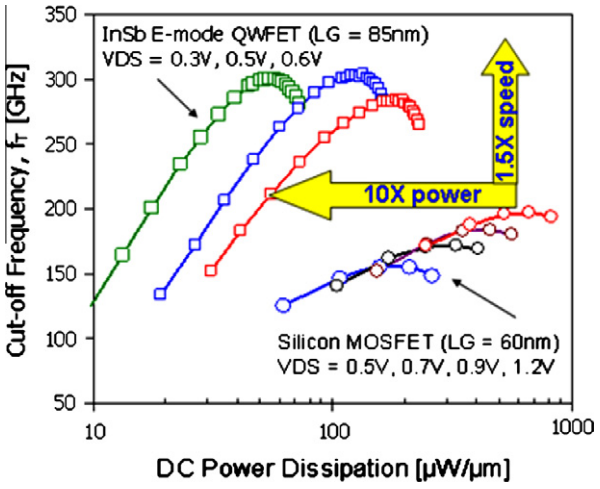

Fig. 1. Plot of cut-off frequency versus dc on-state power from [3] that compares the rf performance of scaled n-channel InSb and Si devices. The former are seen to be better than the latter in terms of both speed and power.

higher mobility heavy-hole band and lowering the density of final states for scattering. Using these strategies with quantum well thicknesses in the range of 5–10 nm and biaxial compressive strains of 1–2%, p-channel mobilities have been raised into the range of 1200–1500 cm^2/V sec as summarized in Table 2 and more thoroughly in [6–9]. Moreover, there is potential for further increases, particularly if one could reach higher strains (especially in GaSb where the best results to date have had strains of only 0.8–1.2% [8]), or could exert *uniaxial* strains as has been done to advantage in SiGe [10] and explored theoretically for the antimonides in [11]. And even the present mobility levels, which are better than the best results in Si (though not Ge), could be sufficient for a future III–V CMOS technology. From the perspective of matching the n- and p-channel devices, the balance is especially favorable if one looks at important high-field and on-state measures like the saturated drift velocity and the density-of-states. With respect to the velocity, for example, the best unity-gain cut-off frequency f_T for a 30 nm n-channel InAs devices is 628 GHz [12], while for a 40 nm p-channel InSb devices it is only a factor of 4 smaller at 140 GHz [6].

Table 2
Material Properties for Three Different Channels.

Quantity	InSb/ (Al,In)Sb	GaSb/ Al(As,Sb)	(In,Ga)Sb/ (Al,Ga)Sb
Mole fraction	Al = 0.35	As = 0.24	In = 0.41, Al = 0.75
Biaxial strain in well (%)	1.9	1.2	2.1
LF hole mob. (cm^2/Vs), well	1230	1350	1500
LF hole mobility, barrier	50	50	50
Saturation velocity (cm/s)	8×10^6	8×10^6	8×10^6
HH/LH effective masses ($\perp$)	0.263/0.015	0.25/0.044	0.26/0.032
DG effective mass ($\perp$)	0.04	0.06	0.057
Schottky barrier (eV)	0.78	1.03	1.0
Band gap (eV), well	0.17	0.62	0.45
Band gap (eV), barrier	0.78	1.66	1.43
Valence band offset (eV)	0.21	0.64	0.43
Dielectric constant, well	17.7	11.6	16.5
Dielectric constant, barrier	15.7	15.7	13

A second advantage of the antimonides is that, as in Si technology, the same material can serve as both an n-channel and a p-channel. To see this we plot in Fig. 2 the cross-channel band diagrams for the InSb, GaSb and InGaSb channels that have achieved the highest mobilities and whose parameters are summarized in Table 2. The calculations were performed using the NEXTNANO program [13] and the particular well/barrier combinations are a 5 nm InSb quantum well with $Al_{0.35}In_{0.65}Sb$ barriers [6], a 7.5 nm GaSb quantum well with $AlAs_{0.24}Sb_{0.76}$ barriers [7], and a 7.5 nm $In_{0.41}Ga_{0.59}Sb$ quantum well with $Al_{0.75}Ga_{0.25}Sb$ barriers [8] where the well thicknesses have been chosen to be consistent with experimental results. The favorable band alignments are evident with the possibility of good confinement of both electrons and holes seen in all three cases, and with the smallest band offsets in InSb. We note that good quality n- and p-channels in the same material layer have already been demonstrated experimentally for InGaSb [14].

The main purpose of this paper is to develop an understanding of the comparative performance and scaling properties of pFETs made with InSb, GaSb or InGaSb as the channel materials. In doing so it should be noted that we do not consider in detail issues related to the gate stack (e.g., MIS designs, gate leakage currents, self-aligned source/drains, etc.), primarily because the relevant non-idealities are less amenable to modeling. Our approach is largely computational, and as reviewed briefly in the next section, the numerical device modeling is done in the density-gradient approximation. The basis for our technology comparisons is then discussed in Section 3. The main results and interpretations appear in Section 4, and the paper closes with some final comments in Section 5.

2. Modeling approach

In modeling the Sb-based pFETs it is important to include the effect of the strong quantum confinement. For this purpose we use the density-gradient (DG) description [15], an approach to quantum transport theory that sacrifices accuracy in the quantum mechanical representation for gains in computational efficiency and facility in modeling other real-world device complications such as complex geometry, self-consistent electrostatics, sophisticated mobility models, generation-recombination phenomena, etc. Because the equations of DG theory have been discussed both in general, and as applied specifically to the problem of hole transport in antimonide pFETs [16], our coverage here can be brief.

For steady-state situations, the relevant differential equations of DG theory can be written as [15]:

$$\nabla \cdot (p\mathbf{v}_p) = 0 \quad p\mathbf{v}_p/\mu_p + p\nabla\psi + p\nabla\varphi_p^{DG} = 0 \tag{1a}$$

$$\nabla \cdot (\varepsilon_d \nabla\psi) = q(N_A - p) \tag{1b}$$

where the generalized chemical potential is given by

$$\varphi_p^{DG} = \varphi_p^{DD}(p) - \frac{2}{r}\nabla \cdot (b_p \nabla r) \quad \text{where } b_p = \frac{\hbar^2}{12 m_p^{DG}} \tag{2}$$

φ_p^{DD} is the ordinary chemical potential of DD theory, $r \equiv \sqrt{p}$, and the coefficient b_p gauges the strength of the DG effect [15]. When the