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Modeling local electrical fluctuations in 45 nm heavily pocket-implanted bulk MOSFET

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ABSTRACT

Modeling local electrical fluctuations on pocket transistor is a challenging task, especially for relatively long gate transistors. Previous work highlighted and qualitatively explain the anomalously high random dopant induced increase of local fluctuations in rather long and heavily pocket device but could not accurately provide the amplitude of the phenomenon. In this paper, a new physical mismatch model is introduced. It is based on the three-transistor model, where one transistor is used to model the channel region and the other two for the pocket regions. This mismatch model provides both qualitative and quantitative mismatch results for all transistor gate lengths and furthermore, it is valid from weak to strong inversion regimes. After the model presentation, a detailed discussion of the qualitative results is performed. Afterwards, the experimental setup is presented. Finally, the physical parameters of the model are characterized and then the resulting level of fluctuations is shown to well model the experimental results.

1. Introduction

MOSFET transistor sizes have been shrunk to deca-nanometers to provide more performance and smaller circuits. But, new problems appeared with the smallest lengths, such as the short channel effect (SCE). Thus, pocket implant technology has been introduced to reduce Vt roll-off and punch-through effects [1–3]. In parallel, the variability between two adjacent transistors has considerably increased and it has become a major difficulty for process development. These local statistical variations are known as mismatch [4] or statistical fluctuations and are generated by many statistical random process fluctuations. Among these fluctuations, the random dopant, the line edge roughness and poly gate granularity have been shown to be the dominant ones in modern CMOS technologies [5]. Matching performances are important for both analog and digital circuits, such as digital–analog converter (DAC) and SRAM respectively, since many blocks are based on the availability of pairs of electrically identical devices [6,7]. To quantify these local fluctuations, Pelgrom et al. [8] introduced a mismatch parameter A_P, where P is an electrical parameter, as threshold voltage, gain factor or drain current. A_P is modeled as (1), where W is the transistor gate width, L is the gate length and $\sigma(\Delta P)$ is the standard deviation of the difference of P between two adjacent devices. This model has physical bases and provides satisfactory accuracy in many cases. However this model is not valid for the whole device geometry range anymore [9–11] because of the SCE and the impact of pockets for rather long lengths. Increased mismatch for short device has been widely observed and was explained by the global increased impurities concentration in the channel [12]. For long lengths, the mismatch was shown not following the Pelgrom's scaling law anymore, and this was attributed to the pockets implants [13,14].

$$\sigma(\Delta P) = \frac{A_P}{\sqrt{WL}} \tag{1}$$

If we plot the scaling law-normalized mismatch $\sigma(\Delta P)\sqrt{WL}$ as a function of the gate length (Fig. 1), we can see the experimental threshold voltage (Vt) mismatch behavior for low power (LP) 45 nm pocket architecture technology. It should be noted that for small gate lengths, Pelgrom's law is followed. For gate lengths higher than 0.1 μm, the normalized mismatch increases, meaning that the scaling law is not followed anymore. Finally, the mismatch decreases for the long transistors, getting closer to scaling law.

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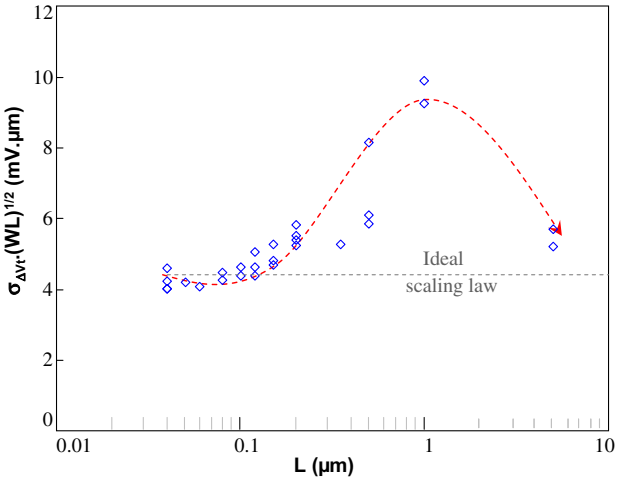

Fig. 1. Experimental mismatch behavior on 45 nm pocket architecture on bulk MOSFET technology. The linear dashed line represents the scaling law.

To understand and to model this Vt mismatch behavior, we started with reviewing the existing Vt models for the pocketed devices. Indeed a valid analysis is necessary for who wants to model the fluctuations for these transistors. Some of the models available in the literature are empirical [15–17]. In addition to those, Ueno et al. [18] developed a complex Vt model, where the basic idea is to introduce an average carrier concentration to determine Vt. He developed this model with five additional parameters: the maximum doping concentration of the pocket profile, the penetration length into the channel, and three enhanced short channel parameters. The sheet carrier concentration is calculated for any Vg, but high accuracy is restricted to the region around threshold condition, which is a drawback for our use, aiming at having a valid model for all gate bias conditions. Cao et al. [19] reported that pocket implant brings anomalously large drain-induced threshold voltage shift and low output resistance to rather long channel devices. He proposed the first physical model of these effects. The additional barrier near the drain creates more DIBL and less output resistance, which are a serious concern for analog design, but not the only one. There are also concerns about pocket implants impact on matching performance. Rios et al. [20] proposed a three-transistor model, which results in a physically compact model, enabling accurate Vt fits for all channel lengths. This model can be approximated by considering a composite device formed by three-transistors in series, with a center device with low threshold voltage bounded by two edge devices with higher threshold voltage, corresponding, respectively, to the channel and to the pockets regions. The pocket-implant impacts the weak inversion, since the device turn-on characteristics are limited by the available carriers in the higher Vt halo region. However, it is valid only in the strong inversion regime. Serrano-Gotarredona and Linares-Barranco [21] proposed a current mismatch model valid for all regions of operation, but on a uniform device. Cathignol et al. [22] show that the rather long devices present strong potential barriers at both source and drain giving these barriers a major role in Vt controlling. Also, as gate biasing becomes higher the barrier height decreases and their ability to control current flow gets lower, making the pocketed device similar to a non-pocketed one. These barriers are responsible for Vt fluctuations. Then, he proposed a physical approach, which provides an adapted model for a correct description of the drain current and the fluctuations level through any Vg bias and for long devices. As the potential barriers totally control Vt independently from the L, the Vt mismatch is also independent on the length and the mismatch keeps constant with increasing length. Thus, if the mismatch is normalized by the square root of the transistor area $\sigma(\Delta Vt)\sqrt{WL}$, it increases with increasing length. However, one of the limitations of this model is that the source/drain peak potential barriers play the same control on channel whatever its length, leading to an indefinitely increase with L. This does not correspond to the behavior observed today, as discussed previously in Fig. 1. Another limitation is that it gives only a qualitative representation of the mismatch. However, the model is not able to quantify the increase based on device parameter and does not provide any explanation for longest devices.

In this context, a new physical mismatch model is proposed here for the first time, aiming at solving this issue. A qualitative representation is obtained and the mismatch behavior is analyzed for different transistor gate lengths and also for different gate biasing conditions. Following, the test structure, the test setup and the extraction method used are explained. In the last section, an accurate characterization of the parameters used in the model is performed. Then the new mismatch model is compared with the experimental results.

2. Mismatch model

A new physical mismatch model is proposed to provide both qualitative and quantitative mismatch representation for all the gate lengths and also in agreement with all gate biasing for pocketed devices. Thus, a model based on the three-transistor series approach is developed to include local Vt fluctuations calculations. One transistor emulates the channel region (ch), whereas the two others in series account for the source and drain pockets (pk) (Fig. 2). The parameters (P_{par}) related to the channel will be noted as P_{ch} and those related to the pocket as P_{pk}.

For the sake of analytical derivation, the inversion charge (Qi) is an approximated version of the one on [23] valid from weak to strong inversion given by (2) for each transistor, where Cox is the oxide capacitance, n is the subthreshold slope parameter, kT/q is the thermal voltage at 300 K, Vg is the gate voltage, Vt_{pk} corresponds to the threshold voltage for a transistor whose channel is homogeneous and highly doped with the pocket doping and Vt_{ch} is the threshold voltage considering only the channel doping.

$$Qi_{par}(Vg) = C_{ox} n \frac{kT}{q} \ln\left(1 + e^{\frac{Vg - Vt_{par}}{n \cdot kT/q}}\right) \quad (2)$$

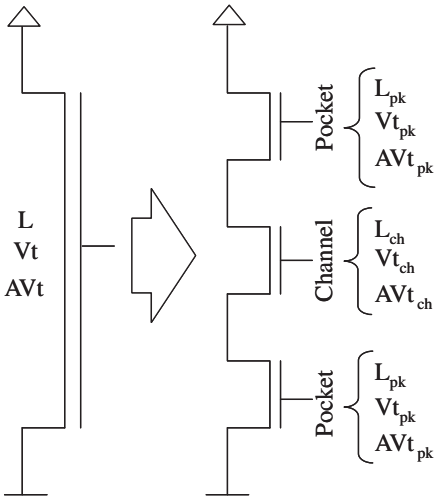

Fig. 2. Three-transistor model. One transistor is to model the channel and the other two for both drain and source pockets.