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Impact of circuit assist methods on margin and performance in 6T SRAM

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ABSTRACT

Large scale 6T SRAM beyond 65 nm will increasingly rely on assist methods to overcome the functional limitations associated with scaling and the inherent read stability/write margin trade off. The primary focus of the circuit assist methods has been improved read or write margin with less attention given to the implications for performance. In this work, we introduce margin sensitivity and margin/delay analysis tools for assessing the functional effectiveness of the bias based assist methods and show the direct implications on voltage sensitive yield. A margin/delay analysis of bias based circuit assist methods is presented, highlighting the assist impact on the functional metrics, margin and performance. A means of categorizing the assist methods is developed to provide a first order understanding of the underlying mechanisms. The analysis spans four generations of low power technologies to show the trends and long term effectiveness of the circuit assist techniques in future low power bulk technologies.

1. Introduction

The 6T SRAM cell design has been successfully scaled in both bulk and SOI down to the 32/28 nm node and has remained for more than a decade the dominant technology development vehicle for advanced CMOS technologies. Reduced device dimensions and operating voltages that accompany technology scaling have led to increased design challenges with each successive technology node. This is especially true for the 6T SRAM cell that often uses minimum device dimensions and requires many waived design rules to achieve its aggressive density targets. Despite these challenges, the 6T SRAM is expected to continue to play a dominant role in future technology generations because of its combination of density, performance, and compatibility with the CMOS logic process. The successful commercial scaling of the 6T SRAM driven by strong industry competition has followed a well defined linear shrink factor of 0.7X over multiple generations, which results in a fairly predictable 2X reduction in cell area per generation. This continued trend in area reduction is accompanied by the well known consequence of increased variance associated with the reduced channel area. Although technology options such as high-*k* with metal gate have provided some relief in variation, the level of integration and functional margins beyond the 28/32 nm generation pose a serious technical challenge.

A unique feature of the 6T SRAM is an inherent trade off between stability when holding data during a read or non-column selected write access and the ability of the cell to be written. This fact means that the device dimensions and threshold voltage targets established for the SRAM devices are a compromise by design. The ability to read and write will be characterized in terms of margins to assess the functional implications. These margins, which we will refer to as write margin (WM), and read static noise margin (RSNM) or static noise margin (SNM), tend to decrease with scaling. Reduced functional margins combined with the growth in bit count and increased variation with each successive generation, lead to a mounting concern for the viability of the 6T SRAM in future generations.

Circuit assist techniques will become increasingly necessary to preserve the 6T cell functional window of operation as scaling con-

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tinues. A range of SRAM functional assist methods have been proposed and discussed [1–23], however there remains no clear agreement in the industry as to which method or combination of methods will emerge as the more optimal solution. While different works compare the assist features in varied settings of technology node and technology type, often little detail is given on the trade offs involved in the selection process. Although power and cost are clearly important factors in determining the optimal assist method, it is first necessary to determine if an assist method will meet the functional margin and delay requirements. Once the assist methods which meet the functional requirements are established, the power and implementation costs can by weighed. The goal of this paper is to provide an approach for assessing the functional effectiveness of the assist methods. A second objective is to explore the impact of CMOS scaling trends on the robustness of various assist methods. The specific contributions of this paper are:

- A margin/delay analysis method is developed for the evaluation of the functional effectiveness of circuit assist methods in 6T SRAM.
- A concurrent analysis across four technology nodes to explore the potential impacts of scaling in low power bulk CMOS technologies.
- A concise overview, and method for categorizing the 6T SRAM assist options.

2. Assist categories

A categorization of the assist methods is introduced to establish a systematic means of characterizing the range of circuit assist techniques used in this discussion. For a given foundry cell design, there are three distinct circuit types or categories to address the reduced window of functionality for the 6T SRAM:

1. Altering noise source amplitude or duration through the access transistor.
2. Modification of the latch strength or voltage transfer characteristics of the latch inverters.
3. Avoidance or masking by design or architecture methods.

While category 3 is included for thoroughness and encompasses a range of approaches including ECC masking or prohibiting the half select issue during a write operation [1], the scope of this work will focus on the bias based methods as defined by type 1 and 2. A categorized summary of the bias based circuit assist methods is shown in Table 1. The assist type given in Table 1 provides the primary mechanistic explanation for the assist method effectiveness.

Table 1
Summary of SRAM circuit assist methods with predominant assist type.

Read assist	Type	Write assist	Type	Terminal(s)
Raise VDD	2	Raise VDD	1	global[a]
Raise VDD at cell	2	Reduce VDD at cell	2	VDDc
Reduce VSS at cell	2	Raise VSS at cell	2	VSSc
WL droop	1	WL boost	1	WL
Reduce Q on BLs[b]	1	Increase (BL–BLB)	1	BL & or BLB
Weaken pass gate NMOS	1	Strengthen pass gate NMOS	1	array PWELL[c]
Strengthen pull-up PMOS	2	Weaken pull-up PMOS	2	array NWELL

[a] VDD applied to terminals VDDc, WL, NWELL (BL and BLB for read, BL or BLB for write).
[b] Reduced voltage or capacitance on BL.
[c] Well bias also modulates pull-down NMOS device in most bulk technologies.

While the category types are useful for quickly analyzing the various assist techniques, they are not fundamentally exclusive, and in some cases both mechanisms influence the net assist effectiveness as we will discuss in more detail in Section 6.

The read and write assist methods listed in Table 1 can and in many cases are used in combination, and most can be implemented in either a static or dynamic mode. The categories can be further distinguished by the voltage terminal or terminals which are manipulated. For example a change in the WL voltage would involve modifying one voltage level while a change in the global VDD would involve changing the voltage on five of the seven available terminals associated with the 6T SRAM cell (VDDc, NWELL, WL, BL and BLB). Increased global VDD is unique for several reasons and will be discussed in more detail in Section 5. Modification of the cell design parameters such as device WL, or device threshold voltage by process change or by means beyond the control of the circuit designer, are outside the scope of this paper.

3. Review of assist methods

A brief overview of circuit assist methods published over the last 5 years will support the objectives of this paper, but the large number of publications prevents an exhaustive review here. It is sufficient for this purpose to provide a sample of the options that have been proposed and to allow us to discuss some of the major advantages and disadvantages in context of the categories and terminal access options given in Table 1.

3.1. Read assist

Those read assist methods we categorize as type 1 include methods that reduce the noise source amplitude or duration, which impact the storage latch. These include those methods we shall refer to as write-back [2–4], reduced word line gate voltage [5–9], increased word line (pass gate) threshold voltage through body bias [10,11], and reduced bit line charge by lowering the voltage or capacitance [3,12–14]. The methods we categorize as type 2, which are intended to improve the resilience of the latch, are increased array VDD [6,15–18], decreased array VSS [7]and reduction in the absolute value of the SRAM pull-up PMOS threshold voltage [10].While some techniques such as write-back (or read–modify–write) are purely dynamic in nature, those techniques which involve altering the well (NWELL or PWELL) bias are proposed as primarily static implementations due to the large RC delay or layout complexity that would be involved in making this technique dynamic. The embodiments proposed as assists in [10,19] are essentially fixed biases set at one point in time to provide some compensation for global variation.

3.2. Write assist

A roughly equal number of publications are invested in the challenge associated with writing the 6T SRAM. The read/write assist symmetry observed from Table 1 is worth noting, and all but one method (increased global VDD) have the not so surprising opposite effect on read stability versus ability to write. Publications that address the challenge of writing the cell following category 1 (increased amplitude or duration of the write signal through the pass gate device) have proposed some form of boost to the word line gate voltage [6,15,20,16] or negative bit line voltage [7,21,9] to increase the VGS of the pass gate device. Those publications that address improving write margin by means of reducing the latch strength include reducing the array supply voltage VDDc [2,5,6,8,