Solid-State Electronics 54 (2010) 1457–1462

Contents lists available at ScienceDirect

Solid-State Electronics

journal homepage: www.elsevier.com/locate/sse

A new vertical MOSFET "Vertical Logic Circuit (VLC) MOSFET" suppressing asymmetric characteristics and realizing an ultra compact and robust logic circuit

Koji Sakui *, Tetsuo Endoh

Center for Interdisciplinary Research, Tohoku University, JST-CREST, Aramaki aza Aoba 6-3, Aoba-ku, Sendai 980-8578, Japan

ARTICLE INFO

Article history:
Received 5 April 2010
Received in revised form 3 June 2010
Accepted 9 June 2010
The review of this paper was arranged by Prof. A. Zaslavsky

Keywords:
Pillar
MOSFET
Vertical
Back-bias effect
Asymmetric characteristics

ABSTRACT

The asymmetric characteristics of the conventional vertical MOSFET are examined. To reduce the *IR* drop influences of the diffusion resistance for the vertical MOSFET, a new vertical MOSFET for the Vertical Logic Circuit (VLC) configuration, which separates the current paths of small currents from large currents, has been proposed.

1. Introduction

Pillar-type MOSFETs were studied for over two decades [1,2], however, recent studies found a more practical, affordable way to manufacture them and extract their performance merits by isolating the pillar body from the substrate with the diffusion region, such as (1) the transistor area reduction for the circuit design, (2) no threshold increase by the back-bias effect, (3) the suppression of the short channel effect, (4) the sub-threshold swing decrease, and (5) the increase in the driving current density [3–6]. A new pillar-type MOSFET, called "a vertical MOSFET", which isolates the pillar body from the substrate with the diffusion, has a promising future device for logic and memory LSIs. With respect to the memory research and development, a number of papers have come up for their application to the three dimensional Flash memories [7–11]. However, due to the device structure of the typical vertical MOSFETs, the top and bottom contacts for the source or drain have different resistances because there is a diffused silicon wiring area in the bottom. Thereby, it has the asymmetric current characteristics [12] between the top and bottom nodes. So far, the impacts on the practical circuit performance with the vertical MOSFETs have not been investigated in details. This paper is devoted to examining the asymmetric characteristics of the conventional vertical MOSFET, proposing a new vertical MOSFET which can suppress the asymmetric characteristics, and validating its impact on an ultra compact and robust logic circuit.

2. Features of vertical MOSFETs

Fig. 1 illustrates the device structure of the vertical MOSFETs. The vertical MOSFET arranges a source, gate, and drain, which make up the silicon pillar vertically. The gate electrode surrounds the silicon pillar and the channel is separated from the substrate by the *n*+ region. Fig. 2 shows the SEM and TEM photographs of the vertical MOSFETs experimentally fabricated with 65 nm CMOS process technology. With its distinct device structure and layout in LSI, the vertical MOSFETs enable a higher performance than the conventional planar MOSFETs. However, the bottom *n*+ region contains the certain resistance to its contact so that this resistance asymmetrically influences on the V_{DS}–I_{DS} characteristics whether the bottom *n*+ is used for the source or drain, as illustrated in Fig. 3a and b simulates the asymmetric characteristics of the vertical MOSFET as follows; transistor size of *W*/*L* is 5 μm/0.18 μm, the gate oxide thickness is 5 nm, and the drain or source resistance of the bottom diffusion line (R_D or R_S) is 100 Ω in this case. The model parameters for the HSPICE BSIM4 simulation are extracted from the experimental data. The drain current in the case that *Source* is bottom diffusion line (R_S) is smaller than in the case that *Drain* is bottom diffusion line (R_D) because the source side resistor lowers not only the effective drain–source voltage of V_{DS} but also the effective gate–source voltage of V_{GS} in the saturated region.

* Corresponding author. Tel.: +81 22 795 5260; fax: +81 22 795 7810.
E-mail address: koji.sakui@cir.tohoku.ac.jp (K. Sakui).

0038-1101/$ - see front matter © 2010 Elsevier Ltd. All rights reserved.
doi:10.1016/j.sse.2010.06.005

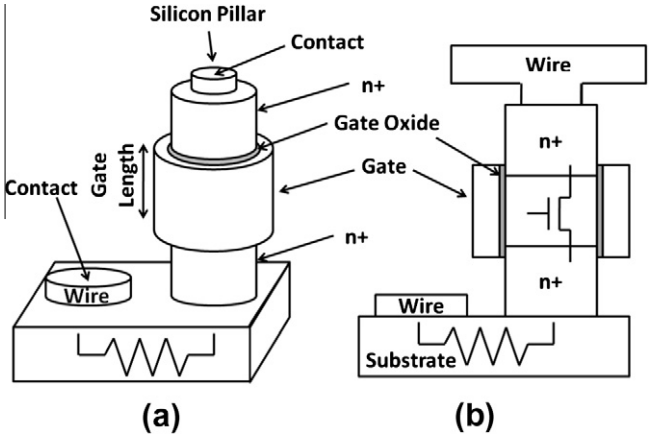

Fig. 1. Bird's eye view (a) and cross-sectional view (b) of the vertical MOSFET. The bottom *n*+ region contains the certain resistance to its contact so that this resistance asymmetrically influences on the device characteristics.

3. A new vertical MOSFETs for logic circuits

Fig. 4 has proposed a new vertical MOSFET, which we name the Vertical Logic Circuit (VLC) MOSFET. The VLC MOSFET can eliminate the *IR* drop influences of the bottom diffused region. Its concept is to separate the current paths by two directions; to the drain of the opposite MOSFET where a large current flows, and to the gate of the next-stage opposite MOSFET where quite a small current flows. The *IR* drop is large to the drain path because of the large current flow while it is much smaller to the gate path due to the small current flow. Fig. 5 shows two stage inverter chain designed by the VLC MOSFETs. Both the drain areas of NMOS and PMOS have two paths to the drain of the opposite MOSFET and to the gate of the next-stage opposite MOSFET. Conversely, Fig. 6 illustrates two types of the conventional vertical MOSFETs inverters; both NMOS and PMOS have the source side or the drain side resistance simply.

4. Simulation results

Fig. 7 shows the simulated inverter gate delay vs. the series resistances of R_D and R_S for two fan-out cases of $F = 1$ or $F = 3$ with the VLC MOSFETs in comparison with that of the conventional vertical MOSFETs. The VLC MOSFET can suppress the *IR* drop so that the gate delay time with the VLC MOSFETs is very close to the case of $R = 0\ \Omega$.

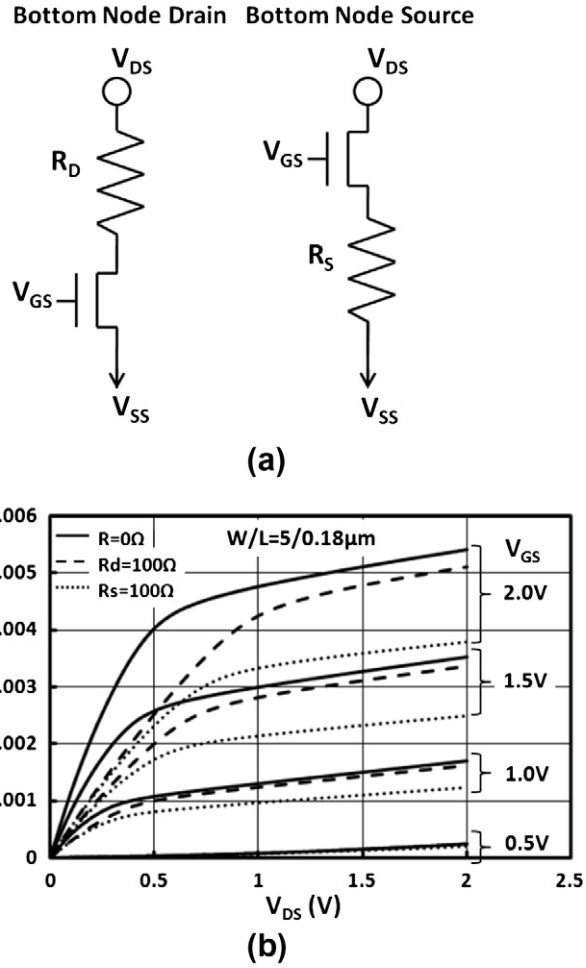

Fig. 3. The vertical MOSFET asymmetric characteristics: (a) Configurations whether the bottom *n*+ is used for the source or drain and (b) The simulated asymmetric V_{DS}–I_{DS} characteristics of the vertical MOSFET.

Fig. 8 simulates the waveforms of the 9-stage inverter ring oscillator for the *Bottom Node Source* case. The source resistances of R_{PS} and R_{NS} are defined as 200 Ω. The PMOS source node of N_{PS} goes down in the V_{OUT} rising due to the *IR* drop of IR_{PS}, and the NMOS source node of N_{NS} goes up in the V_{OUT} falling due to the *IR* drop of IR_{NS}. Thereby, both drain currents of PMOS and NMOS are decreased by not only the reduced drain voltage but also the reduced gate voltage. As a result, the V_{OUT} rising is influenced by

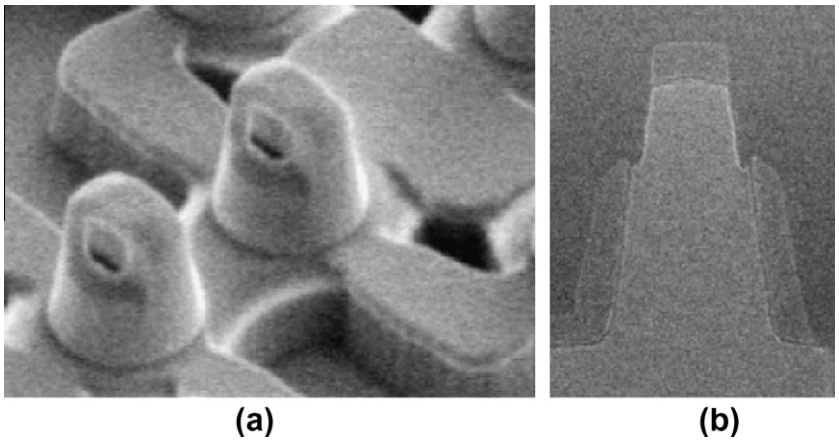

Fig. 2. Microphotographs of the vertical MOSFETs fabricated with 65 nm CMOS process: bird's eye view SEM (a) and cross-sectional view TEM (b).