Solid-State Electronics 54 (2010) 1463–1469

Contents lists available at ScienceDirect

Solid-State Electronics

journal homepage: www.elsevier.com/locate/sse

An analytical model for square GAA MOSFETs including quantum effects

E. Moreno [a], J.B. Roldán [a,*], F.G. Ruiz [a], D. Barrera [b], A. Godoy [a], F. Gámiz [a]

[a] Dpto. de Electrónica y Tecnología de los Computadores, Facultad de Ciencias, Universidad de Granada, 18071 Granada, Spain
[b] Dpto. de Matemática Aplicada, Facultad de Ciencias, Universidad de Granada, 18071 Granada, Spain

ARTICLE INFO

Article history:
Received 12 April 2010
Received in revised form 13 May 2010
Accepted 21 May 2010
Available online 26 June 2010
The review of this paper was arranged by Prof. A. Zaslavsky

Keywords:
Gate-All-Around MOSFET
Quantum mechanical effects
Inversion charge modeling
Inversion charge centroid
Charge confinement
Gate-to-channel capacitance

ABSTRACT

In this paper we introduce an analytical model for square Gate-All-Around (GAA) MOSFETs including quantum effects. With the model developed, it is possible to provide an analytical description of the 2D inversion charge distribution function (ICDF) in square GAA MOSFETs of different sizes and for all the operational regimes. The accuracy of the model is verified by comparing the data with that obtained by means of a 2D numerical simulator that self-consistently solves the Poisson and Schrödinger equations. The expressions presented here are useful to achieve a good description of the physics of these transistors; in particular, of the quantization effects on the inversion charge. The analytical ICDF obtained is used to calculate important parameters from the device compact modeling viewpoint, such as the inversion charge centroid and the gate-to-channel capacitance, which are modeled for different device geometries and biases. The model presented accurately reproduces the simulation results for the devices under study and for different operational regimes.

1. Introduction

Multiple-gate (MuG) MOSFETs are considered a serious alternative for keeping up with the continuous reduction in device dimensions imposed by Moore's law. These structures show promising possibilities in relation to the control of short channel effects (SCEs) and the achievement of ideal subthreshold swing values [1–3].

Making use of technologies based on these new geometries, channel lengths could be shrunk to below 22 nm accordingly to the latest edition of ITRS [1]. In this respect, their capacity to reduce SCEs and the possibility of using undoped channels are essential features for the achievement of this goal. The latter, in particular, is critical since random impurity effects are by no means negligible in nanometric devices [4,5]. These effects produce a dispersion of fundamental parameters such as the threshold voltage and the subthreshold slope [4–7]. Moreover, MuG MOSFETs are part of the Silicon-On-Insulator (SOI) transistor family, which demonstrates unique features that look promising for future mainstream CMOS technologies [6,7]. The use of ultra-thin-body (UTB) and MuG SOI structures allows the fabrication of fully-depleted devices that offer not only extremely good control of SCEs but also a very good behavior with respect to drain-induced barrier-height lowering (DIBL), threshold voltage roll-off, and off-state leakage [6,7].

Both square and cylindrical Gate-All-Around (GAA) MOSFETs are currently under intense study from the simulation and modeling viewpoint [3,8–17]. One key area in these structures is the study of quantum mechanical effects (QMEs), since both structural and electrical confinement (produced by a square gate in the quadruple-gate device and by a circular gate in the cylindrical one) make these devices (nanowires FETs) quasi-1D transistors, where transport occurs in a set of loosely coupled propagating modes.

In this work we focus on square GAA MOSFETs. To the best of our knowledge, these devices have not previously been analytically described in any depth due to their particular geometrical complexities. The concentration of inversion charge close to the corners of the silicon body makes a bi-dimensional description of the inversion charge distribution and other important magnitudes imperative from the compact modeling viewpoint. The analytical description of cylindrical GAA MOSFETs is simpler since the symmetry of the structure around the rotation angle allows a 1D description, accounting for just the radial component [11,13,10,16]. In the case of square GAA MOSFETs, other modeling strategies are necessary.

First, we have introduced an analytical function $f(y,z)$ that accurately reproduces the inversion charge distribution function (ICDF) for square GAA MOSFETs of different sizes and for different biases. The ICDF is related to the inversion charge density as $n(y,z) = N_{inv}|f(y,z)|^2$, N_{inv} (cm^{-1}) being the value of the total electron density integrated over the square area of the silicon channel. Second, we have successfully modeled the inversion charge

* Corresponding author. Tel.: +34 958 244071; fax: +34 958 243230.
E-mail address: jroldan@ugr.es (J.B. Roldán).

0038-1101/$ - see front matter © 2010 Elsevier Ltd. All rights reserved.
doi:10.1016/j.sse.2010.05.032

centroid (ICC) and the gate-to-channel capacitance (C_{GC}), making use of the proposed analytical ICDF. The geometry of these devices makes the definition and modeling of the ICC a tough issue. To deal with this, we have presented a definition that correctly characterizes the spatial distribution of the inversion charge in the silicon channel.

The paper is organized as follows: in Section 2 we describe the main features of the simulator used. We deal with the ICDF modeling in Section 3. The definition, calculation and modeling of the ICC and the C_{GC} are presented in Sections 4 and 5, respectively. Finally, the main conclusions are given in Section 6.

2. Simulator description

The simulation data presented in this work have been obtained by using a simulator developed within our research group [8,12]. The geometry and cross-section of the GAA MOSFET studied is shown in Fig. 1, where t_{ins} and t_{Si} are the insulator thickness and the silicon body thickness, respectively. It can be seen that the gate completely surrounds the square silicon channel where conduction takes place. To reach a fast convergence, the 2D Poisson and Schrödinger equations, the latter solved for each energy valley, have been self-consistently solved using the predictor-corrector scheme proposed by Trellakis et al. [18] including the energy valley degeneration of the silicon conduction band. The simulator achieves accurate results for different structures, materials and gate voltages if the number of energy levels and their corresponding wave functions employed in the calculation is high enough to capture all the occupied levels.

The geometry of the device shown in Fig. 1 confines the electrons in the plane perpendicular to the transport direction, which means that we are dealing with a 1D electron gas. The quantum charge density is therefore obtained by evaluating the following expression [8,18]:

$$\rho(y,z) = \frac{q}{\pi}\left(\frac{2mk_BT}{\hbar^2}\right)^{\frac{1}{2}} \sum_n \Psi_n^2(y,z)\Im_{-\frac{1}{2}}\left(\frac{E_F - E_n}{k_BT}\right)\left[\frac{C}{cm^3}\right] \quad (1)$$

where q is the electron charge, E_F is the Fermi level, Ψ_n is the wave function belonging to energy level E_n, $\Im_{-1/2}$ the complete Fermi–Dirac integral of order $-1/2$ and the remaining symbols have their usual meaning.

The simulator uses finite elements for the discretization of the equations. More details of the code can be found in the following Refs. [8,11,19]. In all the simulated devices, we have considered an undoped substrate ($N_A = 10^{14}\,cm^{-3}$), a metal gate with a work-function of 4.61 eV and an insulator thickness of 1.5 nm. The t_{Si} values considered in our work were 10, 15 and 20 nm.

3. Inversion charge modeling

In this section we propose an analytical model to describe the ICDF of square GAA MOSFETs. As starting point, we used the approach followed by Ge et al. for the symmetrical Double Gate MOSFETs (DGMOSFETs) [20]. Thus, we tried to obtain a 2D analytical model for the ICDF by generalising the 1D eigenfunctions proposed there (Eq. (4) in Ref. [20]). We adapted the quantum mechanical variational calculation employed in [20] for the square geometry corresponding to the GAA MOSFETs considered in this paper, in this way linking the analytical expression of the eigenfunctions to the inversion charge for each gate voltage and device size.

The model obtained with this procedure was compared with the simulation results but it did not fit well for certain gate voltage values and device sizes. The main explanation for this behavior could be the following: the boundary conditions chosen for the electric potential calculation were of Dirichlet kind, using a constant potential value at the semiconductor–insulator interfaces, following the approach presented in [20]. This approximation was good for DGMOSFETs devices because of the one-dimensionality of the structure; however, for a 2D square GAA MOSFETs this is not the case outside the flat band operation regime [8]. More complex boundary conditions would render more realistic results although they would increase the complexity of the analytical models. This extra complexity would make the approach useless from the compact modeling point of view.

Thus, in order to obtain a model analytically simple and accurate enough to reproduce the simulation results for different gates voltages and device sizes, we had to use a different approach. We proceeded to do so by using several trial functions. We found the best results were achieved by making use of the following inversion charge distribution function:

$$f(y,z) = A'\left[\sin\left(\frac{\pi y}{t_{Si}}\right)\right]^{\frac{1}{2}}\left[\sin\left(\frac{\pi z}{t_{Si}}\right)\right]^{\frac{1}{2}}\left(e^{\frac{-b(t_{Si}-y)}{t_{Si}}} + e^{\frac{-by}{t_{Si}}}\right)\left(e^{\frac{-b(t_{Si}-z)}{t_{Si}}} + e^{\frac{-bz}{t_{Si}}}\right) \quad (2)$$

where the normalization of (2) leads to:

$$A' = \frac{\left(1+\frac{b}{\pi}\right)^2 e^b}{t_{Si}\left(b + \frac{b^2}{\pi^2} + \frac{e^b}{2b}\right)} \quad (3)$$

In this way, the electron density can be obtained as $n(y,z) = N_{inv}|f(y,z)|^2$. A heuristic algorithm was developed to determine the value of the b coefficients (i.e., to obtain the dependencies of the b coefficients on the inversion charge and the device size $b(N_{inv}, t_{Si})$). To do this, we calculated and minimized the root mean square error (RMSE) of the simulated and modeled data for the

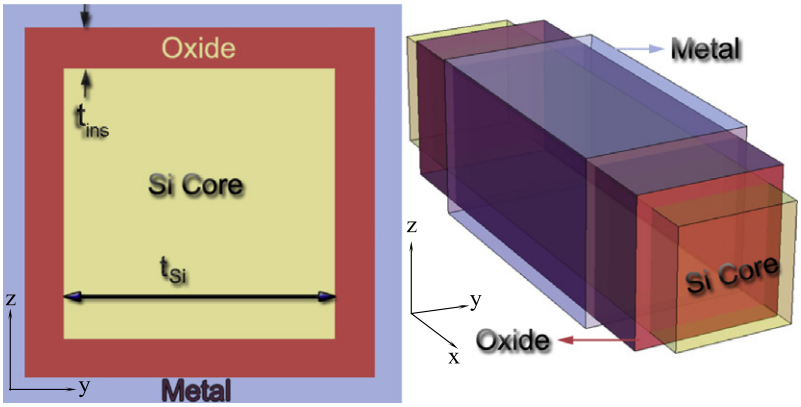

Fig. 1. Cross-section and 3D geometry of the square GAA MOSFETs under study.