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Estimation of amorphous fraction in multilevel phase-change memory cells

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ABSTRACT

The effective thickness of the amorphous chalcogenide part within the active element of a phase-change memory cell is estimated through electrical measurements. Current–voltage characteristics obtained at various intermediate cell states are fitted with the trap-limited subthreshold transport model of [9] and the amorphous part thickness is then extracted. Several cell electrical measures, such as the resistance and the threshold voltage, are shown to closely relate to the estimated parameter. The results serve to further validate the trap-limited conduction model, as well as the series phase distribution hypothesis in the active layer of a phase-change memory cell.

1. Introduction

Phase-change memory (PCM) has emerged in recent years as one of the most promising technologies for future non-volatile solid-state memory due to its excellent features, such as low latency, high endurance, long retention and high scalability [1,2]. In principle, information storage relies on the reversible, thermally-assisted structural phase transformation of specific chalcogenide materials, which form the active element of a PCM cell, between two phases called *amorphous* (the reset state) and *crystalline* (the set state) respectively [3]. The two phases exhibit a very high resistivity contrast, which makes the determination of the cell state straightforward and largely immune to noise and aging effects. Several device concepts as well as programming strategies have been proposed in order to demonstrate the potential of PCM to succeed conventional memory technologies such as FLASH [4,5]. Among other factors, multilevel cell (MLC) operation, namely storage of multiple bits per PCM cell, is a key factor for increasing the memory capacity and thus enhancing the cost-per-bit competitiveness of PCM technology [6,7].

In this paper we present a method for extracting useful cell structural parameters, such as the effective thickness of the amorphous chalcogenide part within the volume of the active phase-change element, as well as important material parameters, such as the average inter-trap distance. The presented method is a valuable characterization tool in order to gain more insight into the structural transformation that takes place during MLC operation, while trap density information is critical for understanding reliability issues that arise due to the resistance drift noise of the amorphous phase [8]. Alternative techniques, such as Transmission Electron Microscopy (TEM), provide accurate structural information at small length scales, but are very tedious and require extensive sample preparation. The development of efficient characterization methods that are based on simple electrical measurements is therefore of high practical value.

In our methodology we adopt the trap-limited transport model of Ielmini and Zhang [9], which describes the electrical transport of an amorphous chalcogenide at the subthreshold conduction regime. Experimental current–voltage (I–V) curves of a PCM cell programmed in various intermediate states, that is different resistance levels between the highest (reset state) and lowest (set state), are fitted to the subthreshold current equation in order to extract the useful structural and material cell parameters. Studies of the low-field cell resistance and threshold voltage as a function of the amorphous fraction, i.e., the effective amorphous layer thickness normalized to its maximum value, are also presented. The results show a good agreement between the measurements and the trap-limited transport model and also reinforce the hypothesis of a series distribution of amorphous and crystalline phases in the volume of a programmed phase-change element [10–12].

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2. Measurement setup and experimental procedure

The memory cells characterized in this work are of the "mushroom" type, with a $Ge_2Sb_2Te_5$ (GST) phase-change element (PCE) sandwiched between top and bottom electrodes. Each cell is connected in series with an nMOSFET access device based on 180 nm CMOS technology [13]. Fig. 1 shows a block diagram of the experimental setup. A high-speed pulse pattern generator with two output channels is used in order to provide the electrical programming pulses at the bit-line (BL) and word-line (WL) of a selected cell on a PCM test-array, while a semiconductor parameter analyzer is used for high precision current and voltage measurements. Switching between the two distinct measurement configurations as well as addressing of the specific cell under test is provided by a programmable high-frequency switch system.

The measurement procedure is illustrated in Fig. 2. Each measurement cycle consists of three steps. In the first step, the memory cell under test is programmed in the reset (high resistance) state. In the second step, the cell is programmed in an intermediate resistance level. In the third and final step, the *I–V* characteristic of the cell is obtained. Programming of the memory cell in different resistance levels is achieved by applying rectangular voltage pulses and using the transistor as a current source. The BL is kept constant at a high voltage and the current through the cell is controlled by varying the amplitude of the WL voltage, that is the voltage at the gate of the access transistor. Fig. 3 shows the current versus gate-voltage characteristic of the access transistor when the drain-voltage is set to 3 V. Reset state programming is achieved by applying a box-shaped pulse at the WL with 4.0 V in amplitude and 50 ns duration. To achieve intermediate resistance levels, variable WL voltage amplitudes from 0 to 4 V are used in steps of 0.1 V and the pulse width is set to 200 ns.

Having programmed the cell in an intermediate resistance level, *I–V* measurements are obtained using the parameter analyzer. A current or voltage ramp is applied at the BL while the transistor is biased in the active region. The current is swept up to a value which is high enough to enable threshold switching, therefore measurements both in the subthreshold conduction regime as well as in the dynamic programming regime are collected. Clearly, the first step of the procedure shown in Fig. 2, namely the programming of the memory cell in the reset state, aims to re-initialize the cell in a known, and in principle consistent, structural state before the application of an intermediate level programming pulse. Alternatively, an appropriate long pulse of moderate amplitude can be applied in order to initialize the cell in the set state.

3. Subthreshold conduction and threshold switching

The principle of non-volatile data storage in PCM is based on two fundamental physical mechanisms, known as *threshold switching* and *memory switching* [3]. Fig. 4 shows the characteristic *I–V* curve of the PCM cell when the latter is programmed in the reset state or in the set state. In the reset state, in which part of the PCE is in the amorphous phase, the cell exhibits a high electrical resistance. With increasing voltage, the current grows exponentially. When a critical threshold voltage, V_{th}, is exceeded,

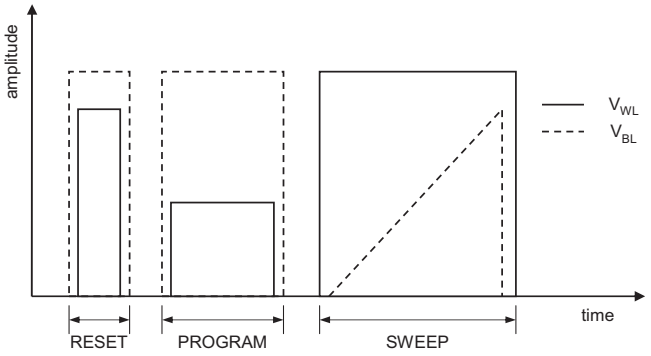

Fig. 2. Measurement procedure: the cell is initially programmed in the RESET state, next it is programmed in an intermediate level, and finally *I–V* data are collected.

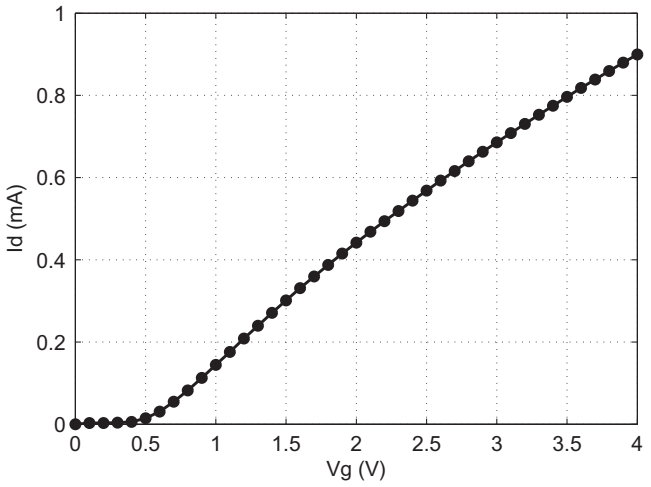

Fig. 3. *I–V* characteristic of the FET access device.

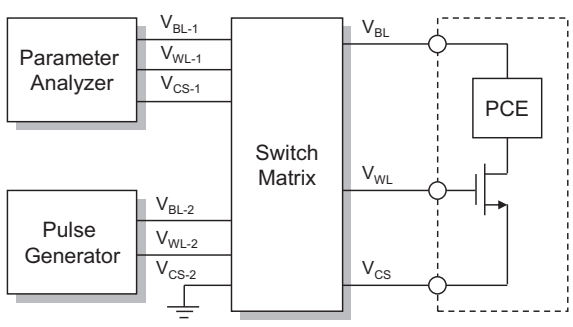

Fig. 1. Experimental setup for PCM cell measurements and characterization using a test-array. Addressing of different cells is provided by the switch-matrix.

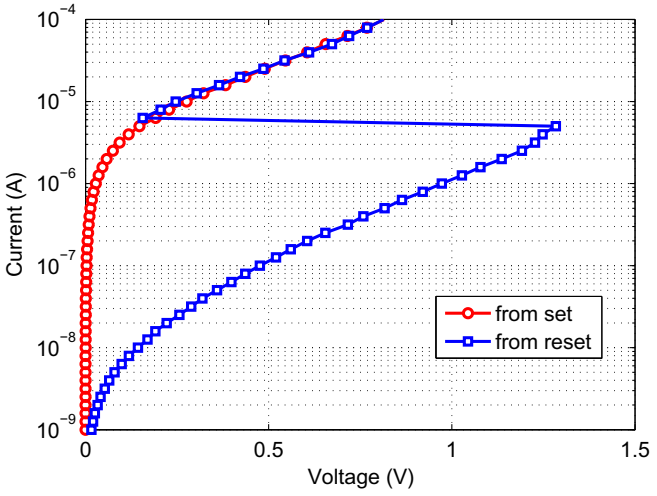

Fig. 4. *I–V* characteristics of the PCM cell programmed in the RESET and SET states. A threshold voltage V_{th} = 1.3 V is observed for the reset state.