Solid-State Electronics 53 (2009) 1246–1251

Contents lists available at ScienceDirect

Solid-State Electronics

journal homepage: www.elsevier.com/locate/sse

Mobility extraction in SOI MOSFETs with sub 1 nm body thickness

M. Schmidt [a,*], M.C. Lemme [b], H.D.B. Gottlob [a], F. Driussi [c], L. Selmi [c], H. Kurz [a]

[a] Advanced Microelectronic Center Aachen (AMICA), AMO GmbH, Otto-Blumenthal-Str. 25, 52074 Aachen, Germany
[b] Department of Physics, Harvard University, 11 Oxford St., Cambridge, MA 02138, USA
[c] DIEGM, University of Udine – IU.NET, via delle Scienze 208, 33100 Udine, Italy

ARTICLE INFO

Article history:
Received 2 June 2009
Received in revised form 9 September 2009
Accepted 10 September 2009
Available online 9 October 2009

The review of this paper was arranged by Prof. S. Mantl

Keywords:
SOI
MOSFET
Mobility
Fully depleted
Ultra thin body

ABSTRACT

In this work we discuss limitations of the split-CV method when it is used for extracting carrier mobilities in devices with thin silicon channels like FinFETs, ultra thin body silicon-on-insulator (UTB-SOI) transistors and nanowire MOSFETs. We show that the high series resistance may cause frequency dispersion during the split-CV measurements, which leads to underestimating the inversion charge density and hence overestimating mobility. We demonstrate this effect by comparing UTB-SOI transistors with both recessed-gate UTB-SOI devices and thicker conventional SOI MOSFETs. In addition, the intrinsic high series access resistance in UTB-SOI MOSFETs can potentially lead to an overestimation of the effective internal source/drain voltage, which in turn results in a severe underestimation of the carrier mobility. A specific MOSFET test structure that includes additional 4-point probe channel contacts is demonstrated to circumvent this problem. Finally, we accurately extract mobility in UTB-SOI transistors down to 0.9 nm silicon film thickness (four atomic layers) by utilizing the 4-point probe method and carefully choosing adequate frequencies for the split-CV measurements. It is found that in such thin silicon film thicknesses quantum mechanical effects shift the threshold voltage and degrade mobility.

1. Introduction

Scaling of CMOS technology beyond the 32 nm node seems questionable using bulk silicon technology. Fully depleted channel transistors such as Fin-field effect transistors (FinFETs) or ultra thin body silicon-on-insulator (UTB-SOI) MOSFETs are considered promising candidates for future CMOS applications. Their advantages are high short-channel-effect (SCE) immunity, nearly ideal subthreshold swing, enhanced current drive, higher I_{On}/I_{Off} ratios and better control of threshold voltages V_{th} [1–4].

A major concern with fully depleted MOSFETs as the silicon film thickness decreases below 10 nm is their high parasitic source and drain series resistance. While this inherent feature may eventually be solved by selective epitaxy and/or silicided source drain leads [5–7], there is an urgent need to extract reliable device parameters even from test devices available today. Inversion channel mobility, in particular, can not be extracted accurately from standard split-C/V [8] and drain current measurements due to the high parasitic source and drain resistance of such MOSFETs, unless specific structures are implemented [9].

For UTB-SOI MOSFETs, a mobility extraction test structure has been proposed that includes additional contacts to the inversion layer [9]. These allow four-point probe measurements of the intrinsic voltage drop across the channel (compare Fig. 1a) and thus eliminate access series resistance. While this mobility test structure has been applied to SOI and strained SOI devices [10,11], it has not yet been tested for ultimately thin channels of a few atomic layers. In addition, the split-CV method requires measuring the gate to channel capacitance. Here, the combination of large access and channel resistance may lead to frequency dispersion effects, similar to the well known effect in conventional MOS capacitors [12]. This must be taken into account when correctly extracting carrier mobility with the split-CV method.

In this article, we demonstrate frequency dispersion during mobility extraction with the split-CV method and discuss its effects for UTB-SOI MOSFETs below 10 nm channel thickness by comparing UTB-SOI, recessed-gate UTB and conventional SOI MOSFETs (compare Fig. 1). We further verify a 4-point probe method for mobility extraction to avoid access resistance issues in UTB devices. Finally, we present mobility data extracted with the 4-point probe method and taking into account frequency dispersion from UTB-SOI *n*-MOSFETs down to 0.9 nm SOI thickness.

* Corresponding author. Tel.: +49 241 8867 232; fax: +49 241 8867 571.
E-mail address: schmidt@amo.de (M. Schmidt).

0038-1101/$ - see front matter © 2009 Elsevier Ltd. All rights reserved.
doi:10.1016/j.sse.2009.09.017

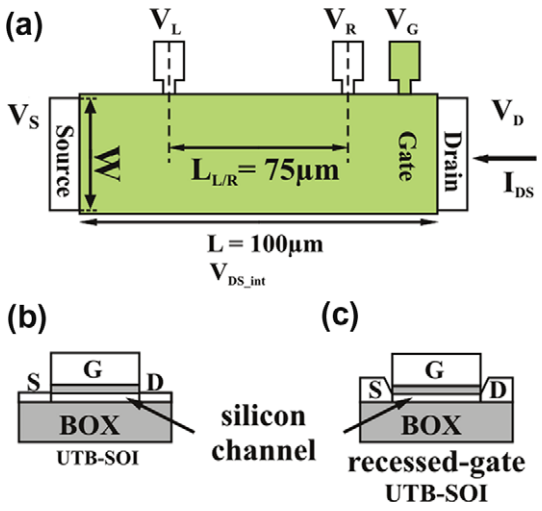

Fig. 1. (a) Schematic top-view of a 4-point probe SOI MOSFET with two additional contacts to the channel ($V_{L/R}$). (b) Schematic cross section of an UTB-SOI MOSFET with a constant silicon thickness across the source, drain and channel. Note that the reference devices are fabricated in a similar manner with a thicker silicon thickness of 50 nm. (c) Schematic cross section of a recessed-gate UTB-SOI MOSFET.

2. Experimental

2.1. Mobility extraction

The effective mobility (μ_{eff}) of a MOSFET is defined in

$$\mu_{eff} = \frac{L}{W}\frac{I_{DS}(V_G)}{V_{DS}Q_{inv}(V_G)} \quad (1)$$

where L and W are the given gate length and gate width and I_{DS} is the measured drain to source current (as a function of gate voltage V_G). Key for the correct extraction of μ_{eff}, however, is the precise knowledge of the internal voltage drop V_{DS_int} across the channel and the measurement of the inversion charge density Q_{inv}. Both V_{DS} and Q_{inv} are strongly affected by high access resistance. Esseni et al. have therefore proposed a specific large area MOSFET with additional contacts to the active channel region [9], as shown schematically in Fig. 1a. For the transistors investigated in this work, we have chosen gate lengths of L = 100 µm and various channel widths of W = 15, 30 and 40 µm. These rather large dimensions minimize the influence of parasitic capacitances. The additional contacts V_L and V_R are spaced 75 µm and enable the currentless measurement of the voltage drop across $L_{L/R}$. This voltage can then be extrapolated to the full voltage drop V_{DS_int} between the physical source and drain with their distance of L = 100 µm.

The inversion charge Q_{inv} can be determined from the inversion charge density N_{inv} by integrating the gate to channel capacitance C_{GC} measured between the shorted source and drain contacts and the gate as (q is the elementary charge) [8].

$$Q_{inv} = qN_{inv} = \int_{-\infty}^{V_G} C_{GC}(V_G)dV_G \quad (2)$$

In the case of a single gate UTB-SOI MOSFET, the effective vertical electric field E_{eff} can be deduced from Q_{inv} according to [13]:

$$E_{eff} = \frac{Q_{inv}}{2\varepsilon_{Si}} \quad (3)$$

2.2. Device fabrication

Three different types of devices with intrinsically different access resistances have been fabricated:

- *conventional SOI MOSFETs*, called "reference" from here on, where the source and drain leads and the silicon channel are 50 nm thick,
- *UTB-SOI MOSFETs*, with constant silicon thicknesses below t_{Si} = 20 nm (Fig. 1b),
- *recessed-gate UTB-SOI MOSFETs*, with channels below t_{Si} = 30 nm, but t_{Si} = 50 nm source/drain leads (Fig. 1c).

Note that the source/drain leads have the same thickness as the channel in both reference devices and UTB-SOI MOSFETs. In the case of recessed-gate UTB-SOI devices, however, the leads are thicker than the channel, which leads to reduced access resistances.

The starting material for all devices was UNIBOND SOI substrate with a Si(1 0 0) active silicon layer and a buried oxide (BOX) thickness of 100 nm. All devices are *n*-MOS type with a boron channel doping level of 1e15/cm^3, i.e. virtually undoped and in (1 0 0) orientation. Initial silicon thicknesses of 50, 20 and 10 nm have been used to fabricate the reference and UTB-SOI MOSFETs (Fig. 1b). For recessed-gate SOI MOSFETs (Fig. 1c), the starting material was SOI substrate with a silicon thickness of 50 nm. For these devices, a LOCOS process with a silicon nitride (Si_3N_4) mask has been used to reduce the thickness of the silicon channel areas only. Repeated thermal oxidation and wet chemical oxide removal has been carried out to realize different silicon thicknesses down to 0.9 nm.

Standard lithography and reactive ion etching (RIE) have been used for mesa isolation of the devices. A gate oxide of t_{Ox} = 8.4 nm has been thermally grown followed by low pressure chemical vapor deposition of 150 nm poly silicon as gate electrode material. The gates have been patterned in a highly anisotropic HBr/O_2-based RIE process with high selectivity to the underlying gate oxide [15,16]. Finally, self aligned arsenic ion implantation has been carried out to form the source, drain and gate regions as well as the contacts to the inversion channel (compare Fig. 1a). The dopants have been activated by rapid thermal annealing at 980 °C for 45 s in nitrogen ambient. Finally a forming gas annealing step has been applied to passivate interface states and oxide charges and to improve device characteristics.

3. Results and discussion

3.1. Body thickness evaluation

The body thickness has been evaluated using CV measurements and transmission electron microscope (TEM) analysis. The CV method, which has been proposed by Chen et al. [17], relies on the accurate decoupling of the gate and silicon capacitances from the buried oxide capacitance. CV measurements between the gate and source/drain contacts for reference and UTB-SOI MOSFETs with 50–10 nm top silicon thickness are shown in Fig. 2a. Without a back gate voltage (V_{BG} = 0 V), the measured inversion capacitance is modulated by the front gate voltage V_G between 4 mF/m^2 and a very low value (due to scale: ~0 F/m^2), which corresponds to the oxide capacitance of the 8 nm thick gate oxide (4 mF/m^2) and to the series of gate-, silicon- and BOX capacitance. However to extract the silicon film thickness from the CV measurement, the gate and silicon capacitances must be decoupled from the BOX. To this end, a back gate voltage has been applied to form an inversion layer at the back interface. The minimum inversion capacitance C_{inv}, i.e. the series capacitance of gate oxide and silicon film, has then been used to extract the respective silicon thickness t_{Si} (for details see e.g. [17]). The resulting body thicknesses t_{Si} have been plotted versus ellipsometry data measured before gate oxide growth (Fig. 2b). The mismatch of 5 nm between electrical and ellipsometric thickness corresponds to the silicon loss during device processing such as wet cleaning and gate oxide growth. The resulting silicon thickness in case of the 10 nm UTB-SOI MOSFET is