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# Dimensional effects and scalability of Meta-Stable Dip (MSD) memory effect for 1T-DRAM SOI MOSFETs

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ABSTRACT

The difficult scaling of bulk Dynamic Random Access Memories (DRAMs) has led to various concepts of capacitor-less single-transistor (1T) architectures based on SOI transistor floating-body effects. Amongst them, the Meta-Stable Dip RAM (MSDRAM), which is a double-gate Fully Depleted SOI transistor, exhibits attractive performances. The Meta-Stable Dip effect results from the reduced junction leakage current and the long carrier generation lifetime in thin silicon film transistors. In this study, various devices with different gate lengths, widths and silicon film thicknesses have been systematically explored, revealing the impact of transistor dimensions on the MSD effect. These experimental results are discussed and validated by two-dimensional numerical simulations. It is found that MSD is maintained for small dimensions even in standard SOI MOSFETs, although specific optimizations are expected to enhance MSDRAM performances.



## 1. Introduction

The DRAM industry is now facing an important crisis caused by the difficult scaling of the storage capacitor. The SOI transistor architecture provides a drastic solution to this issue: the storage capacitor is just suppressed. Indeed, the SOI transistors floating body can be used to store charges [1]. This property has led to an increasing number of single-transistor SOI DRAM (1T-DRAM) concepts [1–9]. In all those variants, the 'ON' state (bit '1') reflects the presence of excess majority carriers in the body which increases its potential and the drain current. The 'OFF' state (bit '0') is characterized by a lower current obtained when the charges are removed from the body.

Various types of memory cells have been proposed and can be differentiated by their 'ON' state programming method: the excess of majority carriers is generated by impact ionization [1], bipolar junction transistor effect [2] or band-to-band (BTB) tunneling [3]. Several companies are competing in the 1T-DRAM arena. In the approach reported by Toshiba, the 'ON' state programming is achieved by impact ionization [4]. This technology is based on Fully Depleted SOI transistors (FDSOI) where the back gate is negatively biased to store the hole charge and adjust the threshold voltage. Bits '0' and '1' are read in strong inversion. A 128 Mb memory array has been demonstrated with a 90 nm technology node. Studies reported by Intel relied on similar programming and reading mechanisms to fabricate FDSOI 1T-DRAM stand-alone cells using a 45 nm logic technology with high-*k* dielectric integration [5]. Reported works from Samsung [6] and Innovative Silicon [7] favoured Partially Depleted SOI transistors, with non-overlapped source/drain regions architecture and highly doped channel, for their 1T-DRAM named Z-RAM. The cell is programmed and read by a bipolar transistor effect, which results in a low-power dissipation and low '0' state current. In all 1T-DRAM approaches, the critical aspects are the retention time for bit '0' and the difference in drain currents necessary to discriminate bits '1' and '0'.

Recently, a novel single-transistor capacitor-less DRAM, named MSDRAM, has been proposed [8,9]. It is based on the Meta-Stable Dip (MSD) effect in fully depleted (FD) transistors, which results

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in a drain current hysteresis (Fig. 1). Fig. 1 shows the device configuration and the typical MSD hysteresis we have obtained for a large (10 μm × 10 μm) FDSOI transistor fabricated on 55-nm-thick SOI film. The MSD effect is a double-gate mechanism, which consists in monitoring, via the back-channel current, the body potential modification induced by the front-gate voltage $V_{G1}$. The back-gate voltage $V_{G2}$ is kept constant, close or higher than the back threshold voltage. The front-gate voltage is swept back and forth from negative to positive values, i.e., the front body/oxide interface varies between strong accumulation and depletion.

The time dependence of the drain current MSD hysteresis originates from the combination of floating-body transients and interface coupling effects in FD MOSFETs [10,11]. For 'direct' or forward $V_{G1}$ scan, the initial front-gate voltage is negative enough (−4 V) to generate majority carriers by band-to-band (BTB) tunneling in the gate-to-drain/source regions. While the body potential is rapidly reaching equilibrium, the electron current flows at the back channel leading to the 'ON' state of the cell. This biasing corresponds to programming bit '1'. Data is read in the memory window (at less negative $V_{G1}$, see Fig. 1b).

The programming of bit '0' occurs naturally during 'reverse' scan. Indeed, the front gate is switched from 0 V to −2 V; the supply of majority carriers (by band-to-band tunneling, drift–diffusion or Shockley–Read–Hall generation) is not sufficient and the body is in *deep depletion*. The back inversion channel is suppressed which corresponds to the 'OFF' state of the cell.

To read the memory cell, a low drain voltage $V_D$ and a front-gate bias $V_{G1R}$ are applied. For the transistor shown in Fig. 1b, $V_{G1R}$ is selected between −3 V and −1.5 V where the difference in drain current $\Delta I_D$ between the 'ON' state and the 'OFF' state is maximal (the memory window). Cell reading is not destructive and the retention time depends on the programmed '0'-state of the cell. Indeed, bit '1' is *stable* as it corresponds to equilibrium. On the contrary, during the 'OFF' state, the system is in non-equilibrium deep depletion and memory refresh is needed for bit '0'. To store the data ('0' or '1' bits) the front-gate voltage is maintained negative and the drain bias is suppressed.

The MSD effect and MSDRAM operation have originally been documented from experiments on large area transistors [8,9]. Numerical simulations have recently demonstrated the scalability of the MSDRAM down to 50 nm gate length [8,9,12]. In this paper, we examine the MSD effect from the experimental and scalability points of view. In Section 2, details about the experimental devices and the measurement conditions are presented. The influence of the applied biases and the scan speed on the MSD window is emphasized in Section 3. In Section 4, we investigate how the channel dimensions (length and width) and the film thickness impact on the MSD hysteresis amplitude and the 'OFF' state retention time. Finally, in the last section, the scaling trends of the MSDRAM in Fully Depleted SOI MOSFETs are discussed based on measurements and simulations. Possible evolutions of the cell architecture will also be proposed.

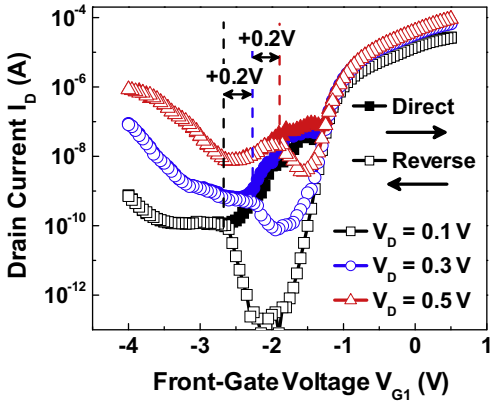


**Fig. 2.** Drain current hysteresis and MSD memory window measured in 55-nm-thick FDSOI MOSFET with channel width and length of 0.5 μm. $V_{G2}$ = 8 V and $V_D$ varies from 0.1 V to 0.5 V.

## 2. Experiment

MSD measurements were performed on standard FDSOI n-MOSFETs fabricated in CEA-LETI laboratories. Unibond SOI wafers with 145-nm-thick buried oxide (BOX) were used. The transistor body was left undoped ($10^{15}$ cm$^{-3}$ intrinsic P-type doping) and the front-gate oxide was 5-nm-thick. The silicon film thickness ($T_{Si}$) was varied from 25 nm to 90 nm by sacrificial oxidation. To reduce the parasitic source and drain resistances, Ni salicidation has been performed. Various channel lengths ($L_G$ from 0.2 μm to 10 μm) and widths ($W$ from 0.2 μm to 5 μm) were investigated to understand the transistor dimensions influence on the MSD effect.

Current–voltage characteristics were recorded at 300 K with an Agilent 4156C analyzer. In order to evaluate the memory window corresponding to the MSD effect, drain-current ($I_D$) measurements versus decreasing (reverse) and increasing (direct) front-gate bias ($V_{G1}$), at several fixed back-gate voltages ($V_{G2}$) were performed. The source was grounded, the drain voltage was kept in the linear region ($V_D$ = 0.1 V) and the back gate was biased in moderate inversion ($V_{G2}$ = 8 V) for all the memory cell operations. Note that this high back-gate voltage value can be drastically scaled down by reducing BOX thickness as discussed in the last section. For the programming and reading curves, the drain current was sampled with a fixed time step of 0.1 s. Measurements were also performed in time domain to probe the 'OFF' state retention time. The programming–reading curves were obtained by applying a pulse at

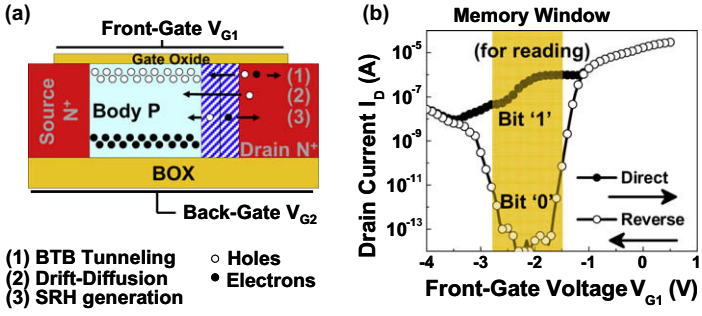


**Fig. 1.** (a) MSDRAM structure and holes injection mechanisms. The BOX thickness is 145 nm and the gate oxide thickness is 5 nm. (b) MSD effect obtained for a 55-nm-thick MOSFET with channel width and length of 10 μm.