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Analytical models of front- and back-gate potential distribution and threshold voltage for recessed source/drain UTB SOI MOSFETs

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ABSTRACT

Front-gate and back-gate potential distributions and threshold voltage of recessed source/drain (ReS/D) ultrathin body (UTB) silicon-on-insulator (SOI) MOSFETs are modeled. The analytical expressions of the front-gate and the back-gate potential distributions are derived by assuming a parabolic potential variation perpendicular to channel and by solving 2D Poisson's equation. Based on strong inversion criterion applied to the surface potential minimum value, threshold voltage model of the short channel ReS/D UTB SOI MOSFETs is derived. The model is verified by comparison with 2D numerical device simulator over a wide range of different material and geometrical parameters and very good agreement is obtained.

1. Introduction

Scaling of conventional bulk CMOS is approaching technological limits [1] and the need for replacement device architecture is growing [2]. Because of its excellent control of short channel effects, a possible alternative to continue the scaling of planar MOSFET is the fully-depleted silicon-on-insulator (SOI) MOSFET with ultrathin silicon-body (UTB) and buried insulator underneath [3–5]. A major problem of the short channel UTB SOI MOSFETs is high series resistance caused by the ultra thin source and drain regions [6,7]. The recessed source/drain (ReS/D) UTB SOI MOSFETs were developed to address this problem by increasing the source/drain thickness, which is achieved by extending the source/drain regions deeper into the buried-oxide (Fig. 1) [8–12].

In comparison with the standard SOI MOSFETs, the special property of the ReS/D SOI MOSFETs is the coupling of the back-side of the silicon-body to the source and drain through the buried insulator. Additionally, these structures still exhibit substrate coupling in the direction perpendicular to wafer surface, but if the buried-oxide thickness (t_{BOX} in Fig. 1) is sufficiently large with respect to channel length, silicon-body predominantly couples from the back-side to the source and drain rather than substrate. Since this condition is satisfied for most of the ReS/D UTB SOI MOSFETs, the existing analytical models for standard fully-depleted SOI MOSFETs [13–17] cannot be applied to ReS/D UTB SOI MOSFETs.

We have developed a simple compact capacitance model for the vertical fully-depleted silicon-on-nothing FET [18], which is also applicable to the ReS/D UTB SOI MOSFETs. The model gives physical insight into the ReS/D SOI operation, but its accuracy is reduced at short channel-lengths.

The aim of this paper is to develop for the first time, a physics-based transistor model for the threshold voltage of the short channel (sub-100 nm) ReS/D UTB SOI MOSFETs, with improved accuracy for all channel-lengths. We derive a general expression for the front-gate surface potential distribution at the gate-oxide-to-silicon-body interface and the back-gate surface potential distribution at the buried-oxide-to-silicon-body interface, that are fundamental for the modeling of SOI MOS devices. These expressions are then used to describe the surface threshold voltage of the ReS/D UTB SOI MOSFETs related to the front-gate and to analyze threshold voltage dependence on various device parameters, such as channel length, gate-oxide thickness, silicon-body

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Nomenclature

C_{BOX}	buried-oxide capacitance
C_{GOX}	gate-oxide capacitance
C_{RSD}	recessed source/drain buried-oxide capacitance
$C_{Si,d}$	fully-depleted silicon-body capacitance
d_{BOX}	length of source/drain overlap over buried-oxide
k_{BOX}	buried-oxide dielectric constant
k_{GOX}	gate-oxide dielectric constant
k_{Si}	silicon-body dielectric constant
K_{BOX}	buried-oxide relative dielectric constant ($K_{BOX} = k_{BOX}/\varepsilon_0$)
K_{GOX}	gate-oxide relative dielectric constant ($K_{GOX} = k_{GOX}/\varepsilon_0$)
L	channel length
N_A	silicon-body doping concentration
N_{ASub}	substrate doping concentration
N_D	drain doping concentration
N_G	gate doping concentration
N_S	source doping concentration
V_{FB1}	front-gate flat-band voltage
V_{FB2}	source/drain-back-gate flat-band voltage
V_{FB3}	substrate-back-gate flat-band voltage
V_{th}	threshold voltage
Φ_M	gate work-function
Φ_{Si}	silicon-body work-function
$\Psi(x,y)$	electrostatic potential in the silicon-body
Ψ_b	difference between Fermi and intrinsic level
$\Psi_{s1}(y)$	front-gate surface potential at the gate-oxide-silicon-body interface [$\Psi_{s1}(y) \equiv \Psi(0,y)$]
$\Psi_{s1}(y = y_{min,s1})$	minimum front-gate surface potential
$\Psi_{s2}(y)$	back-gate surface potential at the silicon-body-buried-oxide interface [$\Psi_{s2}(y) \equiv \Psi(t_{Si},y)$]
$\Psi_{s2}(y = y_{min,s2})$	minimum back-gate surface potential
t_{RSD}	thickness of the source/drain extensions in the buried-oxide
t_{BOX}	buried-oxide thickness
t_{GOX}	gate-oxide thickness
t_{Si}	silicon-body thickness
V_{bi}	built-in potential
V_G	gate voltage
V_{DS}	drain–source voltage
$y_{min,s1}$	position of the front-gate surface potential minimum
$y_{min,s2}$	position of the back-gate surface potential minimum

thickness, channel-doping, and thickness of the source/drain extensions in the buried-oxide.

This paper is organized as follows. In Section 2, the front-gate and back-gate potential distributions are derived. The surface threshold voltage is modeled in Section 3. In Section 4, the accuracy of the threshold voltage model is verified by comparing the model predictions with the 2D device simulation results obtained using Medici [19]. Finally, Section 5 presents some concluding remarks.

2. Potential distribution

2.1. Two-dimensional (2D) Poisson's equation

Before the onset of strong inversion, 2D Poisson's equation in the silicon-body of the ReS/D UTB SOI MOSFETs, shown in Fig. 2, is

$$\frac{d^2\Psi(x,y)}{dx^2} + \frac{d^2\Psi(x,y)}{dy^2} = \frac{qN_A}{k_{Si}} \quad \text{for} \quad 0 \le x \le t_{Si},\ 0 \le y \le L \tag{1}$$

where $\Psi(x,y)$ is electrostatic potential in the silicon-body, N_A is silicon-body doping, k_{Si} is silicon dielectric constant, t_{Si} is silicon-body thickness and L is channel length.

For low values of drain–source voltage V_{DS}, following the study in [13], the potential variation between the front-gate and the back-gate interfaces (x-direction in Fig. 2) can be approximated by the parabolic function

$$\Psi(x,y) = c_0(y) + c_1(y)x + c_2(y)x^2 \tag{2}$$

where coefficients $c_0(y)$, $c_1(y)$ and $c_2(y)$ are functions of y only. Poisson's Eq. (1) can be solved using the following boundary conditions which are specific for the ReS/D UTB SOI MOSFETs:

(1) Continuous electric flux at the gate-oxide-silicon-body interface:

$$k_{Si} \cdot \left.\frac{d\Psi(x,y)}{dx}\right|_{x=0} = k_{GOX} \cdot \frac{\Psi_{s1}(y) - (V_G - V_{FBI})}{t_{GOX}} \tag{3}$$

where k_{GOX} is gate-oxide dielectric constant, t_{GOX} is gate-oxide thickness, $\Psi_{s1}(y) \equiv \Psi(0,y)$ is front-gate surface potential at the gate-oxide-to-silicon-body interface, V_G is gate bias-voltage, $V_{FB1} = \Phi_M - \Phi_{Si}$ is front-gate flat-band voltage, Φ_M is gate work-function, $\Phi_{Si} = \chi_{Si}/q + E_{G,Si}/2q + (kT/q)\ln(N_A/n_i^2)$ is silicon-body work-function, χ_{Si} is electron affinity, $E_{G,Si}$ is silicon bandgap and n_i is intrinsic concentration.

(2) Continuous electric flux at the interface between the buried-oxide and the silicon-body:

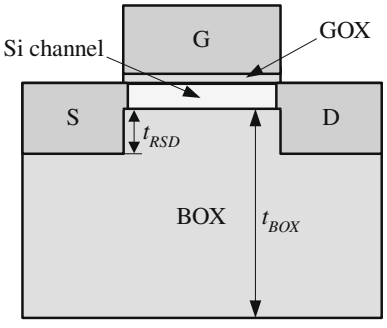

Fig. 1. Recessed source/drain SOI MOSFETs structure cross-section.

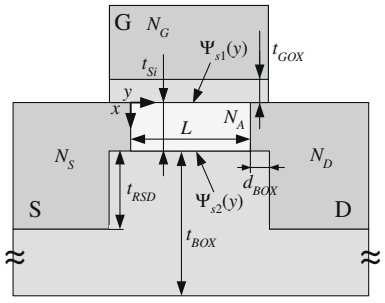

Fig. 2. Recessed source/drain SOI MOSFETs structure close-up with co-ordinate system, device dimensions and interface potentials used for modeling.