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Improvement of operational stability in *SET* states of phase-change-type nonvolatile memory devices using Sb-rich phase of Ge–Sb–Te alloys

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ABSTRACT

For realizing the next-generation phase-change memories (PCM), it is required to reduce the fluctuation of resistance values in *SET* state. The Sb-rich phase of $Ge_2Sb_2Te_5$ was proposed to fulfill the complete crystallization process at each *SET* programming and the PCM devices were fabricated by using the double-layered phase-change materials composed of $Ge_2Sb_2Te_5$ and $Ge_{18}Sb_{39}Te_{43}$. It was found that the *SET* resistances and their fluctuation were reduced as the increase of volume ratio of the $Ge_{18}Sb_{39}Te_{43}$. We can conclude that the compositional modification into the Sb-rich phase can be a good way for improving the *SET* performances for the PCM applications.

1. Introduction

The operational mechanism of the phase-change memory (PCM) is based on the fast and reversible phase-transition of the chalcogenide alloys, in which the memory actions are composed of two operations. One is *RESET*, for which the chalcogenide alloy is melted in an instant by a short electric pulse and then quenched into amorphous state with a higher electrical resistivity. The other is *SET*, for which amorphous phase is crystallized to have a lower resistance by a lower amplitude but longer electric pulse. The reduction of the required current for the *RESET* (I_{RESET}) is one of the most important issues for the phase-change random access memory (PRAM), because a lower I_{RESET} can be absolutely preferable for obtaining a smaller memory cell, which is composed of one PCM device and one access device. On the other hand, the stabilities in *SET* operations, such as *SET* resistance (R_{SET}) uniformity between devices within a single array and small variations of R_{SET} in the same device at each operation, are also very important [1–3], although it has not been focused as a main issue of PRAM so much. One of the main reasons for the *SET* stability degradation is the imperfect crystallization process of phase-change material [4] when the *SET* currents (I_{SET}) having a given pulse width are applied to the PCMs. This incomplete *SET* operation is closely related to the existence of threshold voltage (V_{th}) required for the electronic switching of the chalcogenide alloys. Once the applied voltage across the memory device does not surpass the V_{th}, the electronic switching and successive *SET* process by joule heating cannot be initiated. Because this problem eventually degrades the sensing margin (R_{RESET}/R_{SET}), programming speed, and rewritable endurance, it is strongly desirable to guarantee the complete *SET* processes of the PCM.

Several approaches have been proposed and tried to obtain stable *SET* operations, in which specially-designed *SET* pulse waveforms, such as staircase-down [5], arbitrary slow-quench [6], and two-step *SET* method [7], were proposed. Electrode surface modification was also suggested as an effective method in the reduction of R_{SET} fluctuation [8]. However, these techniques generally require the additional circuit elements or fabrication steps. If we can effectively solve that problem by simply changing the composition of phase-change material, it can be the best way to improve the overall memory functions of the PCM. So far, the searches for new materials have been focused on reducing the I_{RESET} [9–12]. On the other hand, we have proposed the use of Sb-rich nonstoichiometric composition of Ge–Sb–Te-based (GST) chalcogenide alloy for more reliable memory operations of the PCM owing to its distinct

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features such as the direct phase-transition from an amorphous to an *hcp* crystalline phase without the appearance of a metastable *fcc* phase and the improvement of high-temperature stability of the amorphous phase. Phase-transition behaviors of the Sb-rich GST alloy films were confirmed in the X-ray diffraction analysis and four-point probe method as the changes in crystal structures and in sheet resistances, respectively [13]. Although, some problems such as a decrease of crystallization speed [14] and undesirable interdiffusion between Sb added to excess and electrodes [15] were observed, the compositional stability during repetitive rewritable operations and the decrease of threshold voltage V_{th} for electronic switching were confirmed in actual devices employing Sb-rich GST [14]. We expected that this proposed composition could also be more favorable to obtain lower values of R_{SET} without any fluctuation at each *SET* operation. In this work, we investigated the *SET* programming behaviors of the PCM devices employing the Sb-rich GST by using the purposely designed control devices with compositionally modified double-layered phase-change materials. The beneficial effects by using the proposed composition, such as complete *SET* programming and sufficient sensing margin, were successfully confirmed.

2. Experimental details

We fabricated the PCM devices with a typical pore-type structure, which was composed of a bottom electrode (2000 Å-thick TiW), a heating layer (500 Å-thick TiN), phase-change materials, and a top electrode (1500 Å-thick W) in a vertical direction. In this structure, phase-change materials fill the pores patterned into the insulating SiO_2 with the size of 0.5×0.5 μm^2 and was directly contacted to the TiN heating layer [14]. The composition of the phase-change material was $Ge_2Sb_2Te_5$ (GST225) or $Ge_{18}Sb_{39}Te_{43}$. $Ge_{18}Sb_{39}Te_{43}$ corresponds to 22 at.% Sb-excessive phase of the GST225. In this work, the PCM devices employing stacked double-layers with different two compositions of GST225 and $Ge_{18}Sb_{39}Te_{43}$ (Sb22-GST) were also fabricated as controlled devices for comparing their electrical behaviors. These double-layered phase-change materials were prepared by radio-frequency magnetron sputtering method with two targets of GST225 and Sb, in which the sputtering power of 20 W was applied to Sb target only for the deposition of the Sb22-GST. The thickness combinations of the stacked structures (GST225/Sb22-GST) were varied to 2500 Å/500 Å, 2000 Å/1000 Å, and 1000 Å/2000 Å to elucidate the effect of material composition on the *SET* programming behaviors.

The programming behaviors of the fabricated devices were characterized by the measurement system composed of a programmable pulse generator (HP8110A), a semiconductor parameter analyzer (HP4145B), a digital oscilloscope (LeCroy Wavepro7100), and a custom-made semiautomatic measuring software interfaced to PC [14].

3. Results and discussions

Fig. 1a and b shows the programming characteristics for the *SET* and *RESET* operations of the fabricated PCM devices using a single composition of GST225 or Sb22-GST, respectively, when 1000 cyclic signals for the *SET* and *RESET* were repeatedly applied to the devices. The applied pulse widths for the *SET* and *RESET* were fixed at 1 μs and 200 ns, respectively. As can be seen in figures, for the GST225 device, the R_{SET} was fluctuated in the range from approximately 3×10^2 to 4×10^4 Ω. To the contrary, the evolution of R_{SET} during cyclic operations for the Sb22-GST device were very stable and hence the memory margin of approximately 3-orders-of magnitude was well obtained. In these measurements, it is desirable to obtain the constant values in R_{RESET}, so that the next *SET* process could not be affected by different previous crystalline states within the device operating region at each *SET* operation. The voltages with different values of 9 and 6 V for the *RESET* operations were applied to the GST225 and Sb22-GST devices, respectively, which were determined by the typical programming curves of two devices (not shown). Although these values were considered to be sufficiently large for guaranteeing the same initial conditions for every *SET* process, R_{RESET}'s of GST225 device were observed to be somewhat fluctuated (Fig. 1a). It is the case that the *SET* stability of GST225 device can be also improved by optimizing the programming pulse conditions and/or device structures. However, this observed difference between two devices using the same device structure and fabrication process is worthy of discussions. Eventually, imperfect crystallization processes during the *SET* programmings are responsible for the large fluctuation of R_{SET} when the GST225 was employed for the PCM devices.

Two feasible reasons can be explained as follows. The first point is that the composition of GST225 has two crystalline phases (*fcc* and *hcp*) having different crystallization temperature. It can be confirmed for the GST225 that the sheet resistance appears to drop with two-steps at 160 °C and 320 °C with the increase of temperature. The first and second drops reflect the phase-transition from an amorphous to a less conductive metastable *fcc* phase and from an *fcc* phase to a more conductive stable *hcp* phase, respectively [13]. It is possible that these two crystalline phases are simultaneously formed at each *SET* operation with an irregular mixing ratio within the device operating volume, which causes the R_{SET} fluctuation. This phenomenon may remarkably occur especially when an insufficient pulse width is applied for the *SET* operation.

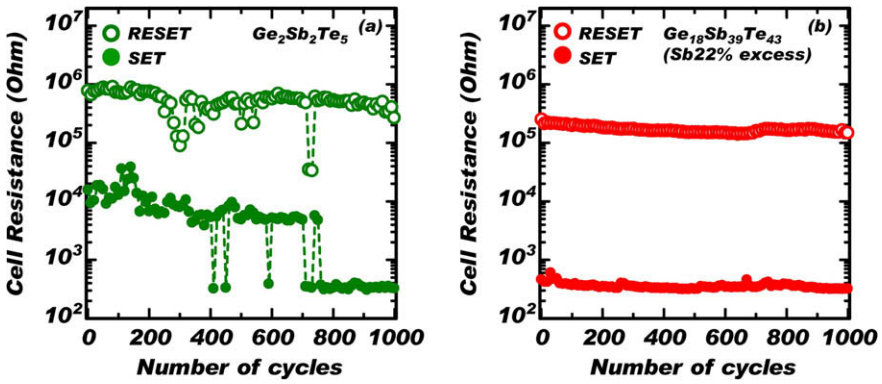

Fig. 1. Variations in R_{SET} and R_{RESET} of the PCM devices using (a) GST225 and (b) Sb22-GST when 1000-times repetitive operations were performed. The pulse amplitudes of *SET*/*RESET* programmings for the two devices were *SET* to be 3 V/9 V and 3 V/6 V, respectively. The pulse widths for the *SET* and *RESET* were fixed at 1 μs and 200 ns, respectively.