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Modeling of the subthreshold current and subthreshold swing of fully depleted short-channel Si–SOI-MESFETs

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ABSTRACT

A model for the subthreshold current and subthreshold swing of fully depleted short-channel Si–SOI-MESFETs is presented in the paper. The subthreshold current of the device is modeled empirically by an exponential function of gate–source and drain–source voltages. The short-channel effects have been included in terms of some empirical constants in the model which have been finally derived from the two-dimensional potential distribution function of the device. The subthreshold swing characteristics of the device are obtained using the subthreshold current model. The validity of the proposed model is shown by comparing the theoretical data with the simulation results obtained by using the ATLAS™ device simulation software.

1. Introduction

The Si-MESFETs fabricated on silicon-on-insulator (SOI) have drawn considerable attention of the researchers for more than a decade [1–6] because of its potentiality as a good contender of Si–SOI-MOSFETs in VLSI/ULSI technology due to the following device characteristics: enhanced radiation hardness, immunity to hot carrier aging, scaling well, and less mobility degradation. Further, the development of a complementary Si-MESFET (C-MESFET) structure similar to the CMOS [7] and the use of mature and well-established SOI CMOS process in the fabrication of SOI-MESFETs in recent times [1] have also enhanced the potentiality of the device for future VLSI/ULSI applications. Moreover, the natural solution to the isolation problems of the SOI technology could make SOI-MESFETs the better choice over the GaAs- and Si-MESFETs for MESFET-based digital VLSI circuits and systems. However, the subthreshold regime of operation of the MESFETs (where the gate electrode of a FET is biased below the threshold voltage) is very important for analyzing the operation of all MESFET-based digital circuits and systems since it represents one of the two stationary stages of the digital circuits. The on-state of the MESFET corresponds to a gate bias above threshold and allows a significant drain current to pass through the device. On the other hand, the off-state corresponds to a subthreshold gate bias when ideally no drain current should pass through the device. In practice, there will always be some leakage current in the off-state owing to a finite injection rate of carriers due to diffusion from the source into the channel. This current in the subthreshold region is an exponential function of the source–channel barrier potential at (i.e. minimum potential at channel–substrate interface) which is very important to analyze the switching characteristics of the device in digital logic and memory applications.

The subthreshold characteristics of conventional GaAs MESFETs were first reported by Chang et al. [8]. This model is practical for circuit simulation because it expresses the drain current as a simple exponential function of the gate voltage. This model is empirical in nature and includes parameters to model most of the important features of MESFET operation in the subthreshold regime. A modified model for the subthreshold current was later presented by Conger et al. [9]. They showed that the drain to source voltage dependence of the subthreshold current in GaAs MESFET is determined by the variation of the threshold voltage due to drain–source voltage and gate–drain diode reverse conduction; and not by drain-induced barrier lowering (DIBL). Based on the Chang's model [8], Marshall and Meindl reported an empirical model for the subthreshold current of short-channel Si-MESFETs [10]. However, only a little works on the subthreshold characteristics of Si–SOI-MESFETs have been reported so far in the literature. Most of the works on SOI-MESFETs mainly deal with the modeling

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of 2D potential distribution and threshold voltage of the device [2–6]. Although, Chiang et al. [5] reported a subthreshold swing model of fully depleted short-channel SOI-MESFETs, the discrepancy between theoretical and simulation results reported in [3] casts some doubt on the validity of their proposed model. Since, the subthreshold characteristics of SOI-MESFETs may be of great interests to many researchers for the designing of SOI-MESFET-based digital circuits and systems; an effort has been made in the present paper to present an empirical model for the subthreshold current of the device for the first time in the literature. The proposed model could be useful for SOI-MESFETs with moderate channel lengths typically above 0.1 μm. The paper also deals with the subthreshold swing characteristics of the short-channel SOI-MESFETs. Such an empirical model may be of great use in the SPICE simulations of various circuits using the SOI-MESFETs.

The subthreshold current is modeled empirically by an exponential function of gate–source and drain–source voltages similar to that of conventional silicon MESFETs [10]. However, the empirical parameters of the expression are analytically derived from the 2D potential distribution function of the short-channel SOI-MESFETs [4] to include the short-channel effects of the device. The subthreshold swing has been obtained from the subthreshold current model discussed above. Finally, the validity of the model is shown by comparing the theoretical results with the commercially available ATLAS™ device simulation software.

2. Theoretical model

The schematic structure of a fully depleted Si–SOI-MESFET under consideration is shown in Fig. 1 where L is the gate-length, t_{si} is the thickness of the active silicon film (i.e. channel thickness), t_{ox} is the thickness of the back oxide layer, V_{gs} is the gate–source voltage, V_{ds} is the drain–source voltage, and V_{bs} is the backside substrate bias voltage. The details of the device parameters and 2D potential distribution function in the channel region of the device are reported elsewhere [4]. The present paper is based on the result of Ref. [4]. It is essential to mention that there are two distinct potential barriers that influence the operation of the device. The channel potential minimum $\psi_{s\min}$ [4] electrically isolates the drain and source and thus confines the subthreshold drain current of the MESFET. It is this channel barrier that is affected by the drain-induced barrier lowering (DIBL) [3–6], the most pervasive effect in short-channel FETs due to 2D electric field distribution in the channel. The other important potential barrier in the MESFET device is the gate barrier that limits the gate current. This gate barrier is not affected by the DIBL phenomenon, and its origin is the main difference between MESFETs and MOSFETs [10]. In case of MESFETs, the gate barrier is a Schottky barrier whereas in MOSFETs, it is a Si/SiO_2 barrier at the gate. However, the subthreshold current of all FETs is mainly described by the diffusion current which can be modeled in the exponential form as

$$I_{ds\text{-}sub} \propto \exp\left(\frac{q\psi_{s\min}}{kT}\right) \tag{1}$$

The channel potential minimum $\psi_{s\min}$ is the minimum value of the bottom potential function $\psi_{bp}(x) = \psi(x,y)|_{y=t_{si}}$ at $Si–SiO_2$ interface, where $\psi(x,y)$ is the 2D potential function obtained by solving the 2D Poisson's equation with suitable boundary conditions as described in Ref. [4]. Using the result of [4], we write

$$\begin{aligned}\psi_{s\min} &= \psi_{bp}(x_{\min}) \\ &= \frac{\beta^2}{2}\left[\frac{\Phi_S \sinh((L-x_{\min})/\delta) + \Phi_D \sinh(x_{\min}/\delta)}{\sinh(L/\delta)} + \gamma\right]\end{aligned} \tag{2}$$

where

$$\beta = \sqrt{\frac{\eta t_{ox} t_{si}^2}{\eta t_{ox} + t_{si}}}; \quad \delta = \frac{\beta}{\sqrt{2}}; \quad \eta = \frac{\varepsilon_{si}}{\varepsilon_{ox}} \tag{3}$$

$$\gamma = 2\left(\frac{\eta t_{ox}(V_{gs} - \Phi_{bi}) + t_{si}(V_{bs} - V_{fb})}{\eta t_{ox} t_{si}^2}\right) + \frac{qN_d}{\varepsilon_{si}} \tag{4}$$

$$\Phi_S = \frac{2V_{bi}}{\beta^2} - \gamma; \quad \Phi_D = \Phi_S + \frac{2V_{ds}}{\beta^2} \tag{5}$$

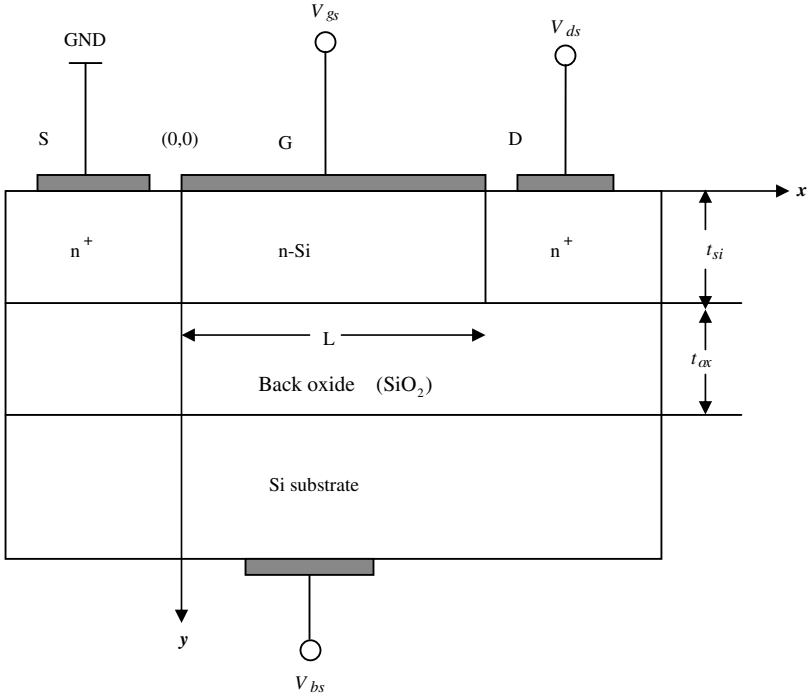

Fig. 1. Schematic structure of a fully depleted Si–SOI-MESFET where where L is the gate-length, t_{si} is the thickness of the active silicon film (i.e. channel thickness), t_{ox} is the thickness of the back oxide layer, V_{gs} is the gate–source voltage, V_{ds} is the drain–source voltage and V_{bs} is the backside substrate bias voltage.