Available online at www.sciencedirect.com
ScienceDirect
Solid-State Electronics 52 (2008) 909–913
SOLID-STATE ELECTRONICS
www.elsevier.com/locate/sse

Normally-off 4H-SiC trench-gate MOSFETs with high mobility

J. Wu [a,*], J. Hu [a], J.H. Zhao [a], X. Wang [b], X. Li [b], L. Fursin [b], T. Burke [c]

[a] SiCLAB, Department of Electrical and Computer Engineering, Rutgers University, 94 Brett Road, Piscataway, NJ 08901, USA
[b] United Silicon Carbide, Inc., 100 Jersey Avenue, Building A., New Brunswick, NJ 08901, USA
[c] US Army TACOM, Warren, MI 48397, USA

Received 10 June 2007; received in revised form 2 November 2007; accepted 10 January 2008
Available online 5 March 2008

The review of this paper was arranged by Prof. Y. Arakawa

Abstract

A new 4H-SiC trench-gate MOSFET structure with epitaxial buried channel for accumulation-mode operation, has been designed and fabricated, aiming at improving channel electron mobility. Coupled with improved fabrication processes, the MOSFET structure eliminates the need of high dose N^+ source implantation. High dose N^+ implantation requires high-temperature ($\geqslant$1550 °C) activation annealing and tends to cause substantial surface roughness, which degrades MOSFET threshold voltage stability and gate oxide reliability. The buried channel is implemented without epitaxial regrowth or accumulation channel implantation. Fabricated MOSFETs subject to ohmic contact rapid thermal annealing at 850 °C for 5 min exhibit a high peak field-effect mobility (μ_{FE}) of 95 cm^2/V s at room temperature (25 °C) and 255 cm^2/V s at 200 °C with stable normally-off operation from 25 °C to 200 °C. The dependence of channel mobility and threshold voltage on the buried channel depth is investigated and the optimum range of channel depth is reported.

Keywords: 4H-SiC; Trench-gate MOSFETs; Mobility

1. Introduction

Silicon carbide (SiC) power devices are expected to drastically outperform Si counterparts due to the superior physical properties of SiC, such as wide bandgap, high breakdown field and high thermal conductivity. In particular, the 4H-SiC MOSFET is a key component in future power switching applications to meet increasing demands of handling higher power densities at temperatures possibly up to 200 °C. At present, however, the development of 4H-SiC MOSFETs has been hampered by notorious channel mobility and gate oxide reliability problems. The major reason for low channel mobility is believed to be the presence of the exponentially increased interface states towards the conduction band edge, resulting in substantial electron trapping and Coulomb scattering at the SiO_2/SiC interface [1]. In addition, interface surface roughness may also play a major role in affecting channel mobility through interface roughness scattering of the electrons. The fact that gate oxide needs to be formed on the source region which usually has a substantial surface roughness due to the heavy dose nitrogen implantation and high-temperature annealing also gives rise to the concerns of gate oxide reliability. Recently, various approaches have been employed to improve the quality of the MOS interface [2–7]. Peak inversion channel mobilities of 50–70 cm^2/V s [3,4] have been obtained by the nitridation of SiO_2/SiC interface through nitric oxide (NO) growth or NO annealing. Even higher inversion channel mobility up to 150 cm^2/V s has been achieved by the use of contaminated alumina environment for gate oxidation [5]. However, there are problems associated with this special process: Rapid thermal annealing for ohmic contacts has to be avoided to attain the above results, or the channel mobility would be degraded by a factor of about two [6]; substantial mobile ions may have

* Corresponding author. Tel.: +1 7324450601.
E-mail address: jianwu@rci.rutgers.edu (J. Wu).

0038-1101/$ - see front matter © 2008 Elsevier Ltd. All rights reserved.
doi:10.1016/j.sse.2008.01.019

been introduced into gate oxide under the contaminated alumina environment [5]. In addition, some researchers utilized a buried channel structure formed by ion implantation to improve the channel mobility in 4H-SiC MOSFETs with up to 140 $cm^2/V\,s$ reported [7]. Similar to [5], however, this high mobility was only obtained without high-temperature ohmic contact annealing, which, however, is an inevitable processing step needed for MOSFET fabrication.

In this paper a 4H-SiC lateral trench-gate MOSFET with a very high channel mobility is reported. Unlike all published works [3–8], the structure of lateral trench-gate MOSFET contains the novel features aiming at improving channel mobility and gate oxide reliability: no N^+ source implantation and hence no high-temperature ($\geqslant$1550 °C) surface-degrading activation annealing are needed throughout the fabrication; no epitaxial regrowth is required; and no MOS channel implantation is performed. It will be reported that truly normally-off MOSFETs under accumulation mode can achieve the high channel mobility of 95 $cm^2/V\,s$ and 255 $cm^2/V\,s$ at room temperature and 200 °C, respectively. As part of a larger on-going effort, results from this lateral MOSFET will be applied towards the fabrication of vertical power MOSFETs aiming at achieving a low specific on-resistance and a stable threshold voltage to ensure that the power MOSFET is truly normally-off over a wide temperature range.

2. Device structure and fabrication

The cross-sectional view of a fabricated 4H-SiC lateral trench-gate MOSFET is presented in Fig. 1. As shown, if the dotted P-type region is converted into N-type by a low dose ion implantation, the lateral structure can be readily transformed into a vertical power MOSFET which can be fabricated without high-temperature, surface-degrading annealing because of the low dose nitrogen implantation [9,10]. The channel length to width ratio of the device is 15 μm/350 μm. The starting 4H-SiC 8° off-axis Si face commercial wafer had an initial 0.22 μm thick N-type epilayer with a doping concentration of $2 \times 10^{16}\,cm^{-3}$ as the buried channel, a 0.90 μm $4 \times 10^{17}\,cm^{-3}$ doped P-type epilayer underneath the channel layer, and a highly doped N^+ cap epilayer (0.15 μm, $N_d = 2 \times 10^{19}\,cm^{-3}$) for implant-free source ohmic contact. The wafer was first etched by inductively coupled plasma (ICP) in the CF_4/O_2 mixture into P-type epilayer for mesa isolation. Thereafter, the trench-gate regions with different depths of the expitaxial buried channel (D_{ch}), namely 0.15, 0.12 and 0.09 μm, were formed by shallow ICP etching. A sacrificial oxide layer was then thermally grown in wet ambient at 1100 °C for 0.5 hr and was stripped off by diluted HF acid. The gate oxide was grown in nitric oxide (NO) at 1175 °C, followed by NO annealing at 950 °C and further oxidation in dry O_2 at 1175 °C plus a final oxidation in NO at 1175 °C, resulting in a total gate oxide thickness of 100 nm. After opening windows into the oxide, 300 nm thick Ni was sputtered to form source and drain contacts. Rapid thermal annealing for ohmic contacts was performed at 850 °C for 5 min in nitrogen forming gas (5% H_2 in N_2), which is a critical step for future vertical power MOSFET fabrication. Gate contacts were formed by 300 nm thick molybdenum.

From the device structure shown in Fig. 1 and the fabrication process outlined, it is seen that source region is formed by epitaxial N^+ layer instead of heavily implanted N^+ region, the high-temperature activation annealing ($\geqslant$1550 °C) is not needed in the fabrication. Hence the preserved SiC surface in gate regions would be more smooth to improve the channel mobility and gate oxide reliability. Although additional low dose implantation will be introduced in the fabrication of vertical power MOSFETs, only low temperature activation annealing (<1550 °C) is required. In addition, the buried MOS channel is formed

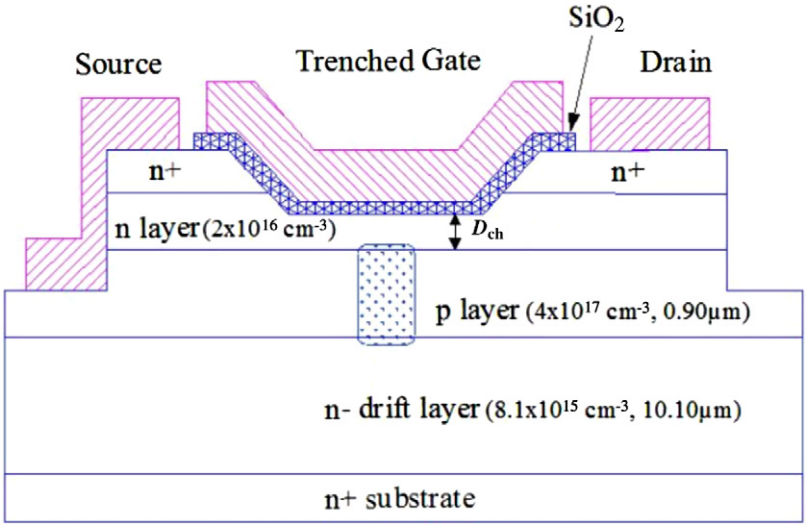

Fig. 1. Cross-sectional view of the lateral 4H-SiC trench-gate MOSFET, which can be readily converted into vertical power MOSFET by converting the dotted p-region into n-region through a lower dose implant with a lower temperature activation annealing.