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Thin-film inverters based on high mobility microcrystalline silicon thin-film transistors

Kah-Yoong Chan [a,b], Eerke Bunte [b], Dietmar Knipp [a,*], Helmut Stiebig [b]

[a] *Jacobs University Bremen, School of Engineering and Science, 28759 Bremen, Germany*
[b] *Research Center Jülich, IEF5-Photovoltaics, 52425 Jülich, Germany*

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Abstract

Thin-film inverters based on high mobility microcrystalline silicon thin-film transistors (TFTs) with different channel lengths were realized. The NMOS enhancement load saturation mode (NELS) inverters were prepared by plasma-enhanced chemical vapor deposition at temperatures below 200 °C. The realization of microcrystalline silicon thin-film inverters facilitates the direct integration of column and row drivers and circuitry on display backpanels. The influence of the transistor properties and underlying contact effects on the performance of the inverters will be discussed.
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Keywords: Thin-film transistors; TFTs; Microcrystalline silicon; Large area electronics; Inverter

1. Introduction

Thin-film transistors (TFTs) are essential components of large area electronic applications like flat panel displays and sensors arrays [1,2]. To date, TFTs based on amorphous silicon (a-Si:H) have established themselves as an inexpensive and reliable technology for display backpanels. However, the realization of more complex peripheral circuitry such as row and column drivers on display backplanes or pixel drivers and circuitries for more advanced display applications like organic light-emitting diode (OLED) displays are not possible due to low material carrier mobility and device stability of a-Si:H [3–7]. So far external drivers are needed or the circuitries have to be realized by polycrystalline silicon (poly-Si) TFTs with high carrier mobilities and stable threshold voltages [1]. However, the fabrication cost of poly-Si TFTs is higher due to high temperature or laser crystallization steps.

An alternative material system, which has been shown high stability for sensor and solar cell applications [8] and superior carrier mobility exceeding 10 cm^2/V s for electrons and holes in the TFTs [9–13], is microcrystalline silicon (μc-Si:H). The advance in terms of carrier mobility and device stability at low temperature (low cost) recommends the material system for more complex electronic circuitries to serve the advanced display applications such as fully integrated display backplanes or OLED displays.

Inverter circuits are the first building block of high performance thin-film large area electronics. Inverters based on poly-Si TFTs realized by thermal annealing of a-Si:H TFTs ($T > 500$ °C) have been presented [14]. Chen et al. and Lee et al. have demonstrated complementary metal-oxide-silicon (CMOS) inverters based on micro or nanocrystalline silicon TFTs [15,16] processed at temperatures of 320 °C [15] and 260 °C [16], respectively. In this paper we present inverters realized by plasma-enhanced chemical vapor deposition (PECVD) at processing temperature of

* Corresponding author. Address: Jacobs University Bremen, School of Engineering and Science, 28759 Bremen, Germany. Tel.: +49 421 200 3570; fax: +49 421 200 3103.
E-mail address: d.knipp@jacobs-university.de (D. Knipp).

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190 °C. The n-channel metal-oxide-semiconductor (NMOS) enhancement load saturation mode (NELS) inverters were realized by using high mobility μc-Si:H TFTs.

The circuit implementation of a NELS inverter is shown in Fig. 1. The input signal is applied to the gate of the drive-TFT, while the gate of the load-TFT is connected to the supply voltage of the inverter, V_{DD}. So the load-TFT operates in saturation region. If the input signal is smaller than the threshold voltage of the drive-TFT, V_{TD}, the input signal of the inverter is considered to be logical low. Under this condition, the load-TFT 'pulls-up' the output voltage to '$V_{DD} - V_{TL}$' representing logical high. V_{TL} is in this case the threshold voltage of the load-TFT. If the input signal (gate voltage, V_G) is larger than '$V_D + V_{TD}$', where V_D is the drain voltage of the drive-TFT, the input signal is considered to be logical high. In this case the drive-TFT operates in linear region and the output signal is 'pulled-down', which corresponds to a logical low. The voltage gain of the inverter is deconvoluted from the slope of the output signal in the transition region from high to low. By definition, the voltage gain of the inverter is described by

$$\text{Gain} = \frac{\partial V_{\text{Out}}}{\partial V_{\text{In}}}, \quad (1)$$

where V_{Out} and V_{In} are the output and input voltage of the inverter, respectively. For an ideal inverter, the voltage gain is defined by the square root of the geometry ratio, β, of the inverter:

$$\text{Gain} = \sqrt{\frac{W_{\text{Drive}} \cdot L_{\text{Load}}}{L_{\text{Drive}} \cdot W_{\text{Load}}}} = \sqrt{\beta}, \quad (2)$$

where W and L are the channel width and length of the constituent TFTs, respectively.

In this paper, we report on the electrical characteristics of μc-Si:H inverters based on NMOS transistors. The influence of the transistor performance and the device geometry on the static behavior of the inverters will be discussed. The underlying contact effect of the high mobility μc-Si:H TFTs on the voltage gain of the inverter will be reported for the first time.

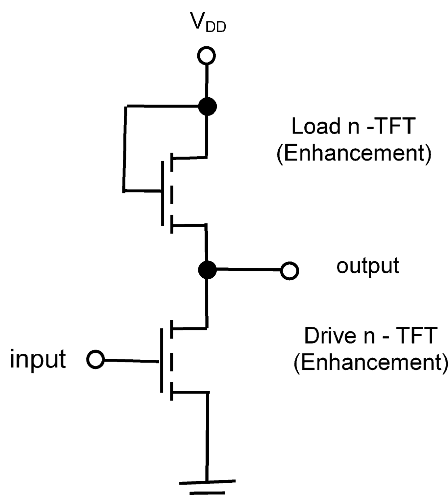

Fig. 1. Circuit of a NMOS enhancement load saturation mode (NELS) inverter. The inverter is realized by combining n-channel microcrystalline silicon thin-film transistors with different channel lengths.

2. Experimental

A schematic cross-section of a top-gate n-channel μc-Si:H TFT is shown in Fig. 2. The drain and source contacts were formed by a chromium layer, followed by a n-type μc-Si:H film deposited by PECVD at 190 °C to form ohmic contacts between the metal electrodes and the channel material. Subsequently a 100 nm thick μc-Si:H intrinsic (i) layer was deposited by PECVD at 160 °C using silane concentration $[SiH_4/(H_2 + SiH_4)]$ of 1%. The film was prepared in the high pressure (1330 Pa) and high power (0.3 W/cm^2) regime to facilitate high deposition rates ($\sim$0.3 nm/s) [17,18]. The i-layer exhibits a crystalline volume fraction of 54%. Under this condition, the highest carrier lifetime of μc-Si:H as a function of crystalline volume fraction was observed [19]. More details concerning the material properties are given elsewhere [20]. The silicon oxide (SiO_2) dielectric of 300 nm thickness was deposited by PECVD at 150 °C. A SiO_2 film was used as gate dielectric to passivate the defects at the μc-Si:H surface and to minimize the defect density of the μc-Si:H/SiO_2 interface [21,22]. Finally, the gate of the TFTs was formed by an aluminum film. The silicon films were patterned using reactive-ion etching, whereas the metal films were structured by wet-chemical etching. The NELS inverters were realized by integrating TFTs according to the circuit implementation shown in Fig. 1. Prior to electrical measurements, all devices were annealed at 150 °C for 30 min under ambient conditions. A detailed discussion of the influence of thermal annealing on the TFT characteristics is reported elsewhere [23].

3. Results and discussion

3.1. Microcrystalline silicon thin-film transistors

The transfer characteristics of a μc-Si:H TFT employed as drive transistor in the NELS inverter are shown in

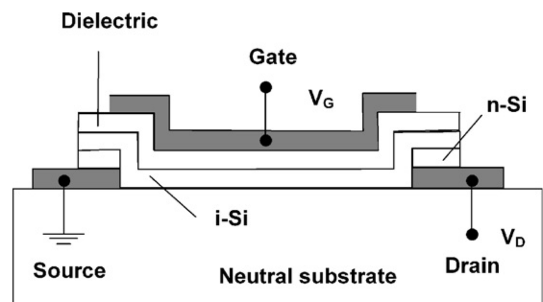

Fig. 2. Schematic cross-section of a top-gate staggered n-channel microcrystalline silicon thin-film transistor.

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