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# Impact of the gate-electrode/dielectric interface on the low-frequency noise of thin gate oxide n-channel metal-oxide-semiconductor field-effect transistors

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**Abstract**

The low-frequency (LF) noise of n-MOSFETs with a 1.5 nm SiON gate oxide is studied for different gate materials, namely, a polycrystalline (poly) silicon gate, a fully nickelsilicided (FUSI) gate and a NiSi FUSI gate deposited on 10 cycles of $HfO_2$. The principal aim is to identify the most likely origin of the predominant $1/f$ noise in the thin gate oxide devices by investigating the impact of the gate electrode processing. It is reported that the lowest input-referred voltage noise spectral density ($S_{VG}$) in linear operation for a gate voltage at the threshold voltage is found for the FUSI transistor, while adding 10 cycles of $HfO_2$ enhances markedly the noise magnitude. The $1/f$ noise characteristic behaves according to the number fluctuations theory so that the results are interpreted in terms of trapping and de-trapping of channel carriers by defects in the gate dielectric layer. Therefore, the marked effect of the gate material is at present ascribed to the different trap density in the vicinity of the gate-SiON interface, which is derived from the LF noise spectra.


*Keywords:* Low-frequency noise; Thin gate oxide; Gate electrode; Carrier trapping; Gate SiON interface; MOSFETs

## 1. Introduction

Device scaling is going hand in hand with a reduction of the gate oxide thickness ($t_{ox}$), pushing it to its practical limit (1.2–1.5 nm) controlled by direct tunneling. To restrict the off-state current enabling low power applications, therefore requires switching over to alternative high-$\kappa$ dielectrics. Although several aspects of these dielectrics have been extensively studied during the last decade, it is also essential to investigate the low-frequency noise performance of the devices. The latter has recently been reviewed by the authors [1].

For the majority of the reported high-$\kappa$ MOSFETs, the LF noise is governed by $1/f$ fluctuations, which classically scale according to a power law $t_{ox}^n$, with $n$ between 1 and 2 [2,3]. The noise origin can be related to three main mechanisms, which have been extensively discussed in the literature. The original McWhorter model associates current noise with fluctuations in the number of carriers, caused by trapping and de-trapping of carriers via defect centers in the gate dielectric [4]. The measurement frequency determines the depth at which the traps in the oxide are probed and can be calculated from the tunnel distance $z$ given by

$$\frac{1}{2\pi f} = \tau_0 \exp(\alpha_t z) \tag{1}$$

where $f$ is the frequency, $\tau_0$ is the time constant at the $Si/SiO_2$ interface ($\sim 10^{-10}$ s) and $\alpha_t$ the electron (or hole)

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wave function attenuation parameter, usually taken $10^8\ cm^{-1}$. Even if account is made for the energy dependence of the oxide traps [5,6], it is obvious from Eq. (1) that for state-of-the-art deep submicron transistors, with a physical oxide thickness in the range 1.2–1.5 nm, the tunnelling distance becomes of the same order or even larger than $t_{ox}$. The latter implies that the traps located at the interface between the gate dielectric and the gate electrode can play a major role. Based on that, one could expect a change in the basic $1/f$ noise mechanism for lower frequencies. The fact that $1/f$ noise is still observed in such components challenges our present understanding of the fluctuations' mechanism and calls for an in-depth study [7].

The current noise $S_I$ may also be dominated by fluctuations in the phonon-scattering controlled mobility of the carriers, in which case the Hooge's empirical noise expression can be applied [8]

$$\frac{S_I}{I_D^2} = \frac{\alpha_H}{fN} \tag{2}$$

with $\alpha_H$ the Hooge parameter and $N$ the total number of free carriers in the channel.

As a change in the number of carriers by trapping/de-trapping will also influence the Coulomb scattering of the carriers and thus the mobility, a correlated-mobility fluctuations model has also been postulated, given by [9,10]

$$S_{VG} = S_{VFB}[1 \pm \alpha_{sc}\mu_0(V_{GS} - V_T)]^2 \tag{3}$$

$S_{VFB}$ is the voltage spectral density $S_{VG}$ at flat-band condition, responsible for the current fluctuations through trapping/de-trapping of channel carriers, $\mu_0$ is the low-field mobility and $\alpha_{sc}$ the scattering coefficient. The difference between the gate voltage $V_{GS}$ and the threshold voltage $V_T$ is called the gate voltage overdrive.

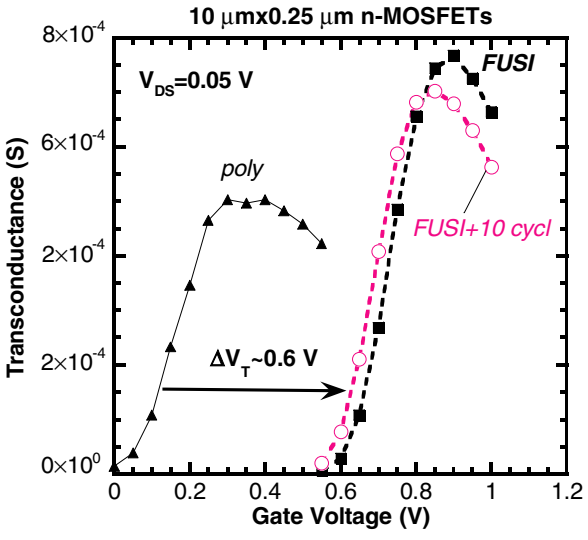


Fig. 1. Transconductance in linear operation ($V_{DS} = 0.05$ V) for a 10 μm × 0.25 μm n-MOSFET corresponding with a polysilicon gate (▲), a NiSi FUSI gate (■) and a NiSi FUSI gate plus 10 cycles $HfO_2$ on top of a 1.5 nm SiON gate dielectric (○).

Table 1
Parameters for the 10 μm × 0.25 μm n-MOSFETs corresponding with the different gate processing conditions. The input-referred noise has been obtained at 10 Hz and 10 kHz, respectively, from the spectra shown in Fig. 3 and corresponding with a gate voltage close to the threshold voltage in linear operation ($V_{DS} = 0.05$ V)

| Gate split | Poly-Si | NiSi | NiSi + 10 cycles |
|---|---|---|---|
| $C_{eff}$ (fF/cm$^2$) | 12 | 18 | 22 |
| $G_{mmax}$ (μS) | 503 | 767 | 702 |
| $S_{VG}$ (μV$^2$/Hz) | | | |
| 10 Hz | 14 | 5.5 | 13 |
| 10 kHz | 0.038 | 0.017 | 0.021 |
| $N_{oteff}$ ($10^{17}$ cm$^{-3}$ eV$^{-1}$) | | | |
| 10 Hz | 7.9 | 6.9 | 24.5 |
| 10 kHz | 21.3 | 21.5 | 38.7 |

This work investigates the LF noise of n-channel metal-oxide-semiconductor transistors with a 1.5 nm SiON gate dielectric and different types of gate material: either n-type polysilicon (poly Si) or FUlly nickel SIlicided (FUSI) in order to verify whether the noise is affected by the gate-electrode/SiON interface. Recently, fully silicided (FUSI) polycrystalline silicon (poly-Si) gates have attracted considerable interest as candidate mid-gap metal gate [11–15]. Among the different silicides, NiSi offers some clear advantages due to its low sheet resistance, low process temperature and limited silicon consumption in the source/drain regions. From a device viewpoint, the replacement of a poly by a FUSI gate provides a clear enhancement of the maximum transconductance $g_{mmax}$, as can be observed in Fig. 1. This is mainly related to the significant increase of the inversion capacitance density ($C_{eff}$), extracted from $I$ to $V$ measurements, as can be derived from the data in Table 1. The increase in the threshold voltage $V_T$ in Fig. 1 by ~0.6 V is related to the 0.6 eV higher work function of the FUSI gate [16]. The Fermi-level pinning below the poly-Si conduction band does not only influence the static device parameters but may also impact the low frequency noise [17].

## 2. Experimental

The impact of the gate material on the LF noise of devices with 1.5 nm SiON as gate dielectric is studied. In order to highlight further the role of the gate-dielectric/gate-electrode interface, some wafers have been processed with 5, 10 or 20 cycles of $HfO_2$ on top of the 1.5 nm SiON, formed by atomic layer deposition (ALD) at 300 °C. All samples received a forming gas anneal for 20 min at 520 °C. The 10 cycles condition corresponds to about half a monolayer, which has a strong impact on the static device characteristics [16–18], as can also be noted from Fig. 1. The reduction in $V_T$ with respect to the FUSI gate device is related to the flatband voltage shift induced by the presence of the $HfO_2$ layer [16,18]. It was recently observed for n-MOSFETs with a poly gate that the $1/f$ noise increases strongly by the presence of 5 or 10 cycles of $HfO_2$ [17].