Available online at www.sciencedirect.com
ScienceDirect
Solid-State Electronics 51 (2007) 252–259
SOLID-STATE ELECTRONICS
www.elsevier.com/locate/sse

Transition from partial to full depletion in advanced SOI MOSFETs: Impact of channel length and temperature

S. Zaouia [a,b,*], S. Cristoloveanu [b], M. Sureddin [a], S. Goktepeli [a], A.H. Perera [a]

[a] Freescale Semiconductor, 850 Rue Jean Monnet, 38926 Crolles, France
[b] IMEP, INPG-MINATEC, 3 Parvis Louis Néel, BP 257, 38016 Grenoble Cedex 1, France

The review of this paper was arranged by Raphaël Clerc, Olivier Faynot and Nelly Kernevez

Abstract

This paper presents a detailed investigation of short-channel effects in advanced partially depleted SOI NMOSFETs. The influence of the back-gate voltage on the threshold voltage reveals the increase of the coupling effect with the channel length. The channel length impact is reversed by using pocket implants. Then SOI devices from the same wafer can behave as fully or partially depleted according to the channel length. This *effective doping* mechanism is amplified at low temperature operation. Systematic measurements show that long channel transistors become fully depleted before short channels, in particular when decreasing the temperature. The reduction of the channel length or the increase of the back-gate voltage and temperature attenuate the gate-induced floating body effect.
© 2007 Elsevier Ltd. All rights reserved.

Keywords: SOI; MOSFETs; Partial depletion; Full depletion; Coupling effect; Low temperature operation; Short-channel effect; GIFBE

1. Introduction

It is clear that SOI technology is the best candidate for future generations of MOSFETs due to multiple advantages [1–3]: scalability, lower junction capacitance, soft error immunity, good vertical isolation, no latch-up, etc. SOI technology is also very attractive for low-power, high-speed applications. Partially depleted (PD) CMOS is currently used for high performance circuits whereas the more scalable fully depleted (FD) devices are expected for the future technology nodes.

The boundary FD/PD is somehow vague because advanced PD MOSFETs can exhibit FD features (residual interface coupling), whereas FD MOSFETs can be converted to PD by back-gate biasing. On the other hand, the transition from PD to FD is not exclusively defined, as conventionally assumed, by the ratio between film thickness t_{Si} and vertical depletion width X_d: $t_{Si} > X_d$ for PD and $t_{Si} < X_d$ for FD. It has been already reported [4] that when scaling down the gate length of SOI transistors, device operation changes from partial depletion (PD) to full depletion (FD) due to the contribution of the source and drain lateral depletion regions. We recently showed that the opposite situation may occur when using pocket implants [5].

In this paper, we take a closer look at this aspect by performing low-temperature measurements. Short-channel effects and gate-induced floating-body effect (GIFBE) in PD SOI MOSFETs are investigated, while considering the impact of the back-gate voltage and temperature. The static parameters, GIFBE and coupling effect are analyzed in advanced N-channel SOI MOSFETs operated at low temperature where full depletion is reinforced. In addition, low-temperature operation is attractive because it yields higher mobility, higher transconductance, higher threshold voltage, lower subthreshold swing and lower junction leakage current [6]. Lowering the temperature to 77 K drops

* Corresponding author. Address: Freescale Semiconductor, 850 Rue Jean Monnet, 38926 Crolles, France. Tel.: +33 4 38922474; fax: +33 4 38922950.
E-mail address: zaouia@enserg.fr (S. Zaouia).

0038-1101/$ - see front matter © 2007 Elsevier Ltd. All rights reserved.
doi:10.1016/j.sse.2007.01.014

the leakage current by two orders of magnitude, while the saturation current increases by 20%.

The paper is organized as follows. In Section 2, a description of the experiment including the characteristics of devices used in this work will be presented. Next, the short-channel effects and coupling effect at room temperature will be discussed (Section 3). Low temperature-effects will be addressed in Section 4. Finally, a typical floating-body effect (GIFBE) in thin oxide MOSFETs will be studied.

2. Experimental conditions

The transistors used in this work have a gate length of 1 μm, 0.1 μm and 40 nm and a width of 1 μm. They were fabricated on 300 mm SOI wafers. The buried oxide (BOX) thickness is 145 nm, and the Si layer is 70 nm thick. The transistors are isolated by shallow trench isolation (STI) and have a 100 nm thick poly-Si gate and a 1.2 nm nitrided gate oxide [7]. They have offset spacer for extension and pocket implant, and a thick nitride spacer. The devices received a high tilt boron pocket implantation. Pocket is a local dopant distribution adjacent to source and drain regions. The channel doping level is about $N_{ch} = 5 \times 10^{17}$ cm^{-3} and the pockets are under-lapping the gate by 80 nm. The high tilt angle pocket implant is used to control the short-channel effect and the off-state leakage, and results in a lower junction capacitance [8]. Also they received lightly doped drain (LDD) implantation which serves to reduce the high electric fields and the hot-carrier injection, thus enhancing the MOSFETs reliability [9]. The source/drain received NiSi silicidation. NiSi has low reaction temperature for salicide formation and offers relatively low sheet resistance [10]. Consequently, NiSi is well integrated in a low temperature process conceived to reduce undesired implant diffusion.

Electrical characteristics of 'partially depleted', non-body contacted, n-channel MOSFETs were studied. Back-gate voltage was varied from −20 V to 20 V, for coupling effect investigation. A large range of temperature was studied, varying from 400 K down to liquid-nitrogen temperature (77 K). All measurements were performed at low drain bias ($V_{ds} = 10$ mV). Attention was paid to parameters such as threshold voltage (V_{th}), mobility, subthreshold swing and transconductance (g_m). V_{th} and the mobility were extracted using the function $Y(V_g) = I_d/\sqrt{g_m}$ which allows suppressing the series resistances [11].

3. Short-channel and coupling effects at room temperature

A main short-channel effect (SCE) is due to the depletion regions of the source and drain junctions, the importance of which increases gradually in deep sub-micron devices. The body depletion, which in long channels was under control of the gate bias, becomes affected by the lateral electric field. As a consequence of this *charge sharing*, the control of the channel by the gate decreases, the threshold voltage (V_{th}) drops, the subthreshold slope degrades and the leakage current increases [3].

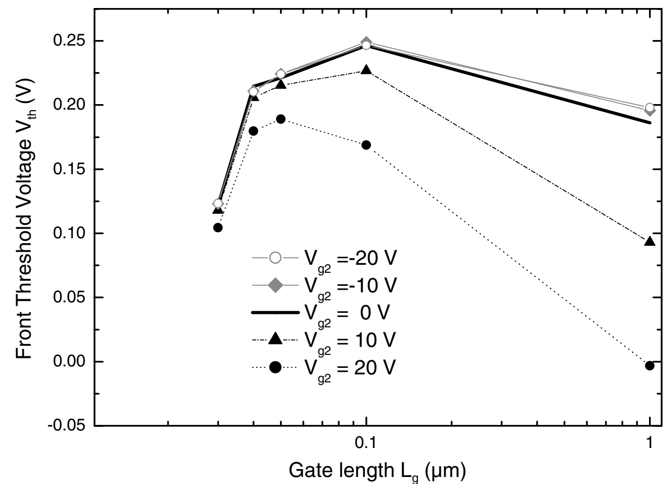

Fig. 1. Front threshold voltage versus gate length for various V_{g2} ($V_{ds} = 10$ mV, $W = 1$ μm, $T = 300$ K).

Boron pocket implantation is widely used to reduce the V_{th} roll-off [12]. Fig. 1 depicts the front threshold voltage versus gate length L_g. It shows a combination of V_{th} roll-up (from $L_g = 1$ μm down to 60–100 nm) and roll-off (for $L_g < 60$ nm). The roll-up is a well-known reverse short-channel effect (RSCE) [5], explained by the modification of the *effective doping* level (N_{eff}) with channel length. Pocket implants are geometrically localized near the source and drain, and result in a local increase of the doping level. As L_g is reduced, N_{eff} increases because the two doping peaks of the pockets tend to merge (Fig. 2), causing V_{th} to increase. On the contrary, in short channels without pocket implants, N_{eff} and V_{th} decrease rapidly when the source/drain charge sharing increases. Fig. 1 indicates that the pockets are effective down to $L_g = 50$ nm, maintaining

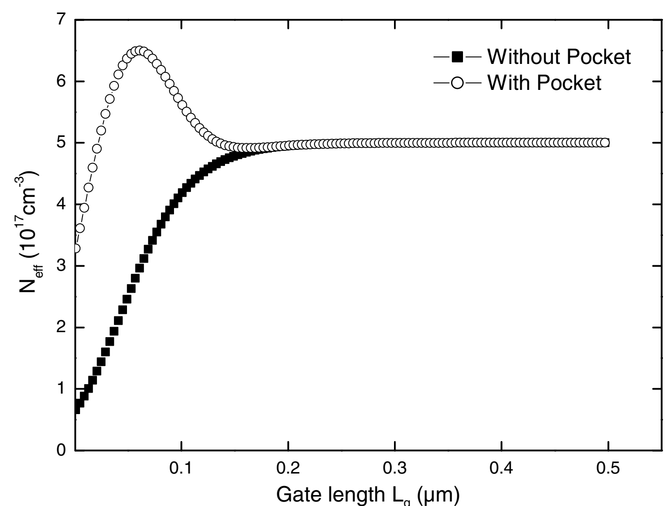

Fig. 2. Effective doping level versus gate length with and without pocket implant, obtained by using [4] and adding the model of the pocket implant in the channel.

Download English Version:

https://daneshyari.com/en/article/753490

Download Persian Version:

https://daneshyari.com/article/753490

Daneshyari.com