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Evaluation of triple-gate FinFETs with SiO_2–HfO_2–TiN gate stack under analog operation

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Abstract

This work presents the analog performance of nMOS triple-gate FinFETs with high-κ dielectrics, TiN gate material and undoped body from DC measurements. Different fin widths and devices with and without halo implantation are explored. No halo FinFETs can achieve extremely large gain and improved unity gain frequency at similar channel length than halo counterparts. The FinFETs with 110 nm long channel achieve an intrinsic gain of 25 dB. Extremely large Early voltages have been measured on long channel nMOS with no halo and relatively wide fins compared to the results usually reported in the literature. The large Early voltage obtained suggests that the devices operate in the onset of volume inversion due to the low doping level of the device body.
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Keywords: FinFET; Analog operation; Triple-gate; Volume inversion; Intrinsic gain; Early voltage

1. Introduction

Double-gate transistors are known to be one of the most promising technological solutions for achieving high-performance sub-100 nm Si MOSFETs [1]. Among the solutions technologically available nowadays the FinFET is considered as an excellent option as it is easily accommodated in a standard silicon-on-insulator (SOI) process [2]. Fig. 1 presents a cross-section view of the FinFET indicating the channel length (L), the fin height (H_{Fin}) and the fin width (W_{Fin}).

In the literature, information can be found on the technological aspects of FinFET fabrication [2] and on the performance of these devices in digital applications indicating a quasi-ideal subthreshold slope, the ratio between on-to-off current and the good control of short-channel effects [3]. Some recent publications address the performance of this promising structure in analog applications [4–7]. According to these studies, FinFETs have an enormous potential to be applied in analog circuits, especially when the devices are operating under volume inversion, leading to extremely large Early voltage values (larger than 1000 V) for a 10 μm long device [5,6]. In Refs. [5,6] devices with doped bodies and nitrided gate oxide were explored whereas in Ref. [7] only no halo devices with $W_{Fin} = 25$ nm were studied.

FinFETs can operate either as a double-gate structure or as a triple-gate device. For double gate operation

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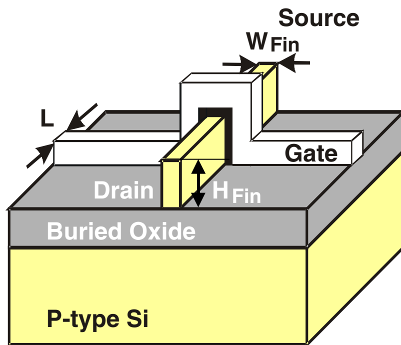

Fig. 1. Schematic representation of a FinFET.

narrow fins are typically used and there is no conduction from the top. For the triple-gate approach there is also a current contribution from the top gate and wider fins can be used [8]. These devices have good scaling perspectives.

The MOSFET scaling implies the use of extremely thin gate oxides, whereby the associated tunnel current can change the device dynamic operation [9]. The technological solution for this problem is the implementation of high-κ dielectrics such as, e.g. HfO_2. To overcome polysilicon depletion affecting the equivalent oxide thickness (EOT) high-k gate stacks with metal gate electrodes as TaN and TiN are presently being pursued [10].

This paper studies the analog operation of triple-gate n-type FinFETs with HfO_2 gate dielectric, TiN gate and undoped body. The most common analog figures of merit as the transistor intrinsic gain, the unity gain frequency and the transconductance-to-drain current ratio are discussed taking in consideration the presence of halo implantation and fin width.

2. FinFET structure

The triple-gate FinFETs were fabricated starting from SOI wafers with 145 nm buried oxide thickness, following the process described in Ref. [11]. The top silicon layer thickness, which is the fin height, is decreased down to 60 nm. After the silicon film definition a 1 nm thick interfacial thermal oxide is grown followed by the atomic layer deposition (ALD) of 2 nm HfO_2 (40 cycles) leading to 2 nm EOT. Subsequently, a 5 nm thick TiN ALD film is deposited and a 100 nm polysilicon capping layer completes the gate stack. The gate patterning is done using 193 nm immersion lithography with resist and oxide hard mask trimming. No channel doping is applied during the processing. After the gate stack definition devices with and without halo (or pocket) tilted implantation have been fabricated. The source and drain extensions are performed using tilted implantation. Nickel silicidation is used for the device electrodes. The channel length (L) of the measured transistors ranges from 50 nm to 10 μm. For 10 μm long transistors fin widths (W_{Fin}) of 22 nm and wider were explored in order to verify the impact of W_{Fin} in the output characteristics. For the rest of the measured transistors two different fin widths (W_{Fin} of 120 nm and 370 nm) were studied.

The digital characteristics of this technology have been reported in Ref. [11], showing the capability of obtaining operational $L = 50$ nm transistors for digital applications.

3. Results and discussion

Prior to exploring the analog properties of scaled transistors we first investigated the operational conditions of long channel devices. The threshold voltage (V_T) of nMOS transistors has been measured using the double derivative technique [12] applied to the drain current (I_{DS}) *versus* gate voltage (V_{GF}) with a drain bias (V_{DS}) of 0.1 V. For the 10 μm transistors (with and without halo) V_T is in the order of 0.35 V. As no channel doping is used, the TiN gate stack efficiently controls the V_T by the adjusted metal workfunction.

The low field carrier mobility (μ_0) and the absolute Early voltage ($V_{EA} \cong I_{DS}/g_{DS}$, g_{DS} being the drain output conductance measured in saturation) values for 10 μm transistors as a function of W_{Fin} are presented in Fig. 2. For the V_{EA} extraction a gate voltage overdrive ($V_{GT} = V_{GF} - V_T$, V_{GS} being the gate voltage) of 200 mV and $V_{DS} = 0.65$ V

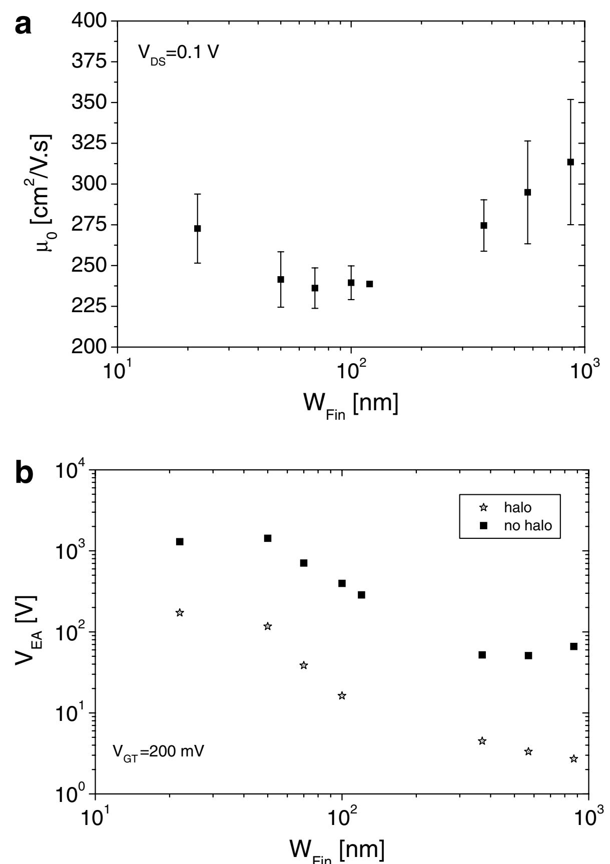

Fig. 2. Extracted (a) low field mobility ($V_{DS} = 0.1$ V) and (b) Early voltage ($V_{GT} = 200$ mV) for 10 μm long FinFETs as a function of the fin width.

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