Available online at www.sciencedirect.com
ScienceDirect
Solid-State Electronics 50 (2006) 1822–1827
SOLID-STATE ELECTRONICS
www.elsevier.com/locate/sse

Behaviour of TFMS and CPW line on SOI substrate versus high temperature for RF applications

M. Si Moussa [a,*], C. Pavageau [b,c], D. Lederer [a], L. Picheta [b], F. Danneville [b], N. Fel [c], J. Russat [c], J.-P. Raskin [a], D. Vanhoenacker-Janvier [a]

[a] *EMIC, Microwave Laboratory of UCL, Place du Levant, 3, 1348 Louvain-la-Neuve, Belgium*
[b] *IEMN-UMR CNRS 8520, Cité Scientifique, 59652 Villeneuve d'Ascq, France*
[c] *CEA-DIF, BP 12, 91680 Bruyères-le-Châtel, France*

Received 20 July 2006; received in revised form 10 October 2006; accepted 10 October 2006

The review of this paper was arranged by Prof. A. Zaslavsky

Abstract

Practical application of integrated circuits requires operation over a wide temperature range. In the case of microwave monolithic integrated circuits (MMICs), the quality of the interconnections as well as the passive matching networks in term of losses is predominent. Therefore, there is a need to investigate the performances of transmission line structures on Si-based substrates in a wide temperature range, as a function of frequency. The behaviour of 50 Ω thin film microstrip (TFMS) and coplanar waveguide (CPW) transmission line topologies on both standard and high resistivity silicon-on-insulator (SOI) substrates versus high temperature is presented.
© 2006 Elsevier Ltd. All rights reserved.

Keywords: CMOS; MMIC; Silicon-on-insulator; TFMS; CPW; Standard and high resistivity; High-temperature effect

1. Introduction

Large scale commercial applications, such as cellular communications require substrates that are low-cost, easy to manufacture and capable of being integrated with digital technologies. Silicon substrate is a good candidate for these applications even if it suffers from dielectric losses. Some applications such as well logging, avionics, and automotive require electronic circuits capable of operating at temperature up to 300 °C. The capability of SOI circuits to expand the operating temperature range of integrated circuits up to 250 °C has been demonstrated [1,2], thanks to its buried oxide (BOX) as well as the fact that the transistor channel is defined in thin silicon layer. Indeed, SOI MOSFETs present lower leakage currents than bulk devices at high temperature, as well as a smaller variation of threshold voltage with temperature. They are also immune to temperature-induced latchup. As a result, SOI circuits can operate at temperatures above 300 °C, while bulk CMOS is usually limited to 150 °C [1,3]. In [4], authors have analyzed the impact of high-temperature operation on the RF performance of a travelling wave amplifier (TWA). They have demonstrated that the losses induced in the passives are the main contributor to the TWA gain and bandwidth degradation at high temperature.

One of the main challenges in the silicon process is no longer high performance transistors but ultra low loss passives, and especially transmission lines for achieving higher frequency and gain performances [1].

On-chip transmission lines can be implemented using thin film microstrip (TFMS) or coplanar waveguide (CPW) lines in a multiple metal layers CMOS technology. Both

* Corresponding author. Tel.: +32 10 47 80 99; fax: +32 10 47 87 05.
E-mail address: simoussa@emic.ucl.ac.be (M. Si Moussa).

0038-1101/$ - see front matter © 2006 Elsevier Ltd. All rights reserved.
doi:10.1016/j.sse.2006.10.008

configurations were built on 130 nm SOI CMOS process modelled through full-wave EM simulations with HFSS Ansoft software environment [5].

In next sections, the behaviour of both transmission line topologies, TFMS and CPW, versus frequency and temperature is presented and compared. These transmission lines were built on standard and high resistivity silicon-based substrates.

2. Methodology

On-wafer measurements were performed, with an Anritsu 37369A™ vector network analyzer. Temperature control is provided by a Temptronics 8-in temperature chuck up to 250 °C. Ground-signal-ground (GSG) (100 μm-pitch) high frequency coplanar Z Probes from Süss™ have been used for signal measurement. The measurements were done over the temperature range from 25 to 250 °C.

In order to extract the transmission lines parameters such as the attenuation coefficient and the characteristic impedance, we performed a two steps calibration. The first calibration step consists in defining the measurement reference planes at the CPW probe tips. This is performed in measuring standards on an alumina substrate and applying the so called LLRM (line-line-reflect-match) calibration technique.

After this first calibration step, the reference planes move at the end of the probe tips, and the reference impedance is equal to 50 Ω. The second step consists of a TRL (thru-reflect-line) calibration in order to withdraw the metallic access CPW pads and then determine the characteristics of the TFMS and CPW lines made on the silicon-wafer, in term of attenuation coefficient and thus lineic losses. The latter step is repeated for each temperature value.

3. Thin film microstrip lines

TFMS are made of a metallic strip, lying on a thin dielectric layer above a ground plane. TFMS were realized on high resistivity (HR) and standard resistivity (STD) SOI wafers. Six copper layers and one extra aluminium (Alucap) layer were available on the 130 nm SOI process of ST-Microelectronics. In our study, the TFMS lines were implemented using the upmost 0.9-μm-thick metal 6 layer as signal conductor, and metal 1 and metal 2 layers stacked together to form the ground plane. The total dielectric layer thickness is 2.9 μm. It is composed of a multilayered structure of silicon dioxide and silicon nitride spacers, as shown in Fig. 1.

We have drawn four TFMS structures with different widths as summarized in Table 1. For each TFMS dimension, a thru line, a short and an open have been designed. These structures allow the extraction of the losses using a thru-reflect-line (TRL) de-embedding method [6].

The lines are designed to have a characteristic impedance of 50 Ω. Fig. 2 shows a typical TRL calibration kit in TFMS implemented on SOI substrate.

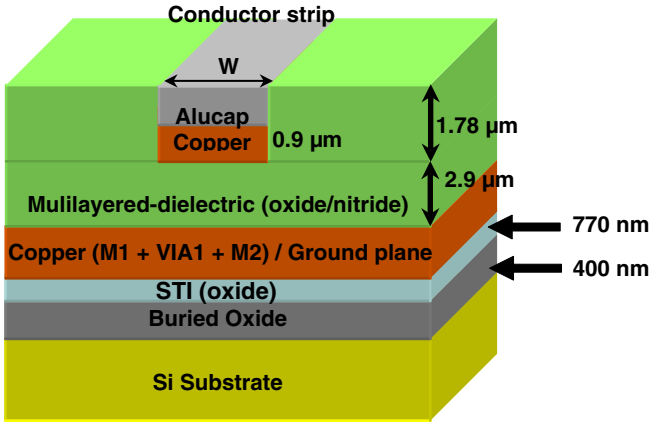

Fig. 1. Geometry of the designed TFMS.

Table 1
The drawn TFMS structures

TFMS structures	Conductor strip width, W (μm)
M6 + Alucap	7
M6	7
M6	2
M6 + Alucap	5
M6 + Alucap	9

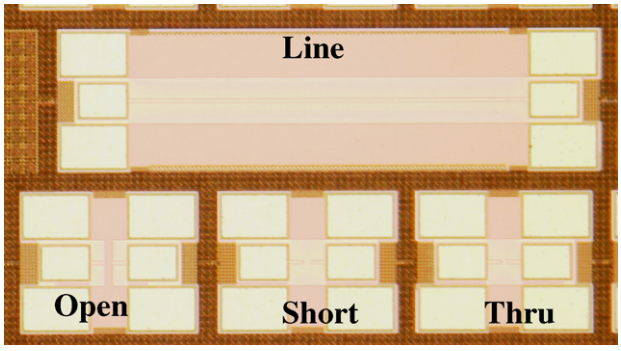

Fig. 2. Chip microphotograph of the designed TFMS calibration kit.

The standards are embedded in CPW to strip line transitions for on-wafer measurement purpose. These access CPW pads as well as these transitions are withdrawn from the measured S-parameters in using the TRL calibration method.

Fig. 3 shows the losses versus frequency for various available TFMS geometries. The lineic losses are defined as the ratio of the real part of the propagation constant ($\gamma = \alpha + j\beta$) and the length of the line. As expected, the line losses increase with the reduction of the conductor width.

Two versions of the 7 μm-wide TFMS structures were designed, for one the signal conductor is made only in metal 6 and the other in stacking metal 6 and an extra Al layer (Alucap) of 0.88 μm.

The use of the Alucap layer enables a reduction of 33% of the losses at 20 GHz.

In TFMS, the back ground plane shields the Si substrate and therefore avoids coupling between the signal and the

Download English Version:

https://daneshyari.com/en/article/753598

Download Persian Version:

https://daneshyari.com/article/753598

Daneshyari.com