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# Howling reduction by analog phase-locked loop and active noise control circuits

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ABSTRACT

This paper proposes a howling reduction circuit using analog phase-locked loop (PLL) and active noise control (ANC) circuits. The proposed circuit reduces howling by generating a signal opposite in phase to howling. To make a signal with the same frequency as howling, we employed the PLL circuit. The ANC circuit was used to control the amplitude of the signal. In addition, we employed pseudo-lock avoidance and differential switch circuits to avoid noise generation. The results confirm the effects of howling reduction by the proposed circuit.



## 1. Introduction

Howling is a source of noise in acoustic systems, and techniques for howling reduction have been proposed by researchers [1–6]. These techniques typically employ digital circuits with analog/digital (A/D) converters and digital/analog (D/A) converters. In general, both the processing time periods in digital circuits and the latencies in the converters are significant. Some of the reported techniques [1–3] take more than 0.5 s before howling reduction is achieved. Such a slow operation is not adequate because human ears detect howling noise within milliseconds. Furthermore, a few techniques [4–6] predict howling signals and can reduce howling within 10 ms of operation. However, the prediction used in these techniques assumes that the howling frequency is dependent only on the distance between the microphone and speaker. In actual acoustic system environments, sound reflections are significant and their prediction is not possible. Therefore, howling reduction techniques that operate at high speed and do not rely on prediction must be established.

In contrast to digital circuits, analog circuits generally operate at high speed. We previously proposed an active noise control system with analog circuits and have demonstrated high-speed operation to cancel noise in a duct [7]. This active noise control circuit (ANC) controls the amplitudes of signals to cancel noises without any prediction. Therefore, it has the potential to reduce howling noise. However, this ANC cannot control the signal phase adequately, and thus, to effectively cancel noises, additional circuits are required to control the phase of signals [8]. In this paper, we propose a phase-locked loop (PLL) for controlling phase and frequencies, and, by using both the PLL and ANC, we demonstrate howling reduction by circuit simulations.

## 2. Configuration of howling reduction circuit and simulation of each part

We employed the simulation program HSPICE for the circuit simulator with the Onsemi Sanyo 0.8 μm CMOS process rule. In acoustical systems, a sound is input to a microphone and the signal from the microphone is amplified. Then, the amplified signal is output by a speaker, which is fed back to the microphone through an acoustical path and this feedback signal causes howling. To emulate the howling, we employed a resistance and capacitance (RC) oscillation circuit shown in Fig. 1. Signals *input*, *output* and $O_{ps}$ in the circuit are defined in this figure. Amp in Fig. 1 indicates an amplifier, while the phase shift comprises the RC shown in Fig. 2. Add1 indicates an adder circuit. In this RC oscillation circuit, *input* is amplified by Amp and the resulting *output* is fed back with a delay due to the phase shift and superposed to *input* by Add1. At the frequency corresponding to the delay period, a gain from this RC oscillation circuit becomes infinity, and thus howling appears in *output*. Hereafter, signals obtained from this RC oscillation circuit are regarded as 'without (w/o) control'. A block diagram of the proposed howling reduction circuit is shown in Fig. 3 along with the RC oscillation circuit, and signals $I_{hrc}$, $O_{mul}$, $O_{lpf}$, $O_{pll}$, $O_{del}$ and $O_{anc}$ in the circuit are also defined. In this proposed circuit,

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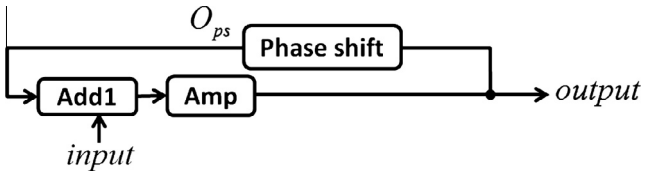


**Fig. 1.** Block diagram of RC oscillator.

from the output of Amp $I_{hrc}$, the PLL generates a signal with the same frequency as the howling signal in $I_{hrc}$. Because output from PLL $O_{pll}$ is led 90° from $I_{hrc}$, we used a circuit shifting the phase of the signal by 90° (90° delay). ANC adjusts the amplitude of the output of the 90° delay $O_{del}$ to that of the howling. The output of the ANC $O_{anc}$ is superposed to the howling signal in $I_{hrc}$ by an adder circuit Add2. This configuration using only the PLL, 90° delay and the ANC can typically reduce howling. However, the PLL does not necessarily output signals with the same frequency as the howling. To suppress signals with frequencies different from that of howling, we also implemented the pseudo-lock avoidance and differential switch circuits, shown in Fig. 3. Results obtained from the configuration in Fig. 3 are regarded as 'with control'. We describe details of each block in the following.

### 2.1. PLL

PLLs are commonly employed to synchronize the frequency of an output signal with that of an input signal [9]. A PLL comprises a phase comparator (PC), a low-pass filter (LPF) and a voltage-controlled oscillator (VCO). For the PC, a multiplier is employed in most cases, and it generates output voltage corresponding to the phase difference between two signals, the input and feedback from the VCO. The LPF removes high frequency noise from the PC output. The VCO is an oscillator with an output frequency controlled by the LPF output. The VCO output is used as an output of the PLL and is also fed back to the PC.

Various types of VCOs in PLLs have been proposed for different applicable oscillation frequencies [10–15], and those VCOs output signals with different duty ratios. For our purpose, oscillation at a kHz band is required. In addition, if we define the duty ratio $D$ as

$$D = \frac{T_+}{T_+ + T_-} \times 100[\%] \quad (1)$$

where $T_+$ is the time of positive value and $T_-$ is the time of negative value of the signal; $D$ should be 50%. This is because the howling frequency is kHz and the $D$ of howling is 50%. Therefore, we adopted a VCO with the kHz band with a $D$ of 50%, shown in Fig. 4. In Fig. 4, $V_b$ = 1 V which oscillates the VCO at a free-running frequency. $V_{dd}$ and $V_{ss}$ are voltage sources with 2.5 V and −2.5 V, respectively. We simulated the operation of this VCO, and obtained the dependence of output frequencies ($O_{pll}$) on the input ($O_{lpf}$) voltage, as shown in Fig. 5. The oscillation frequencies of the VCO were in the kHz band and were proportional to $O_{lpf}$. $D$ was ∼50% at any of the frequencies.

A wide-range Gilbert multiplier (WRM) is used for the PC [16], and a circuit diagram of the LPF adopted here (cut-off frequency = 26 Hz) is shown in Fig. 6. To check the operation of the PLL comprising these PC, LPF and VCO components, we input a sine wave with an amplitude of 1 V and a frequency of 4 kHz to $I_{hrc}$, and the resulting $I_{hrc}$ and $O_{pll}$ are shown in Fig. 7. We confirmed that $O_{pll}$ oscillates at the same frequency as $I_{hrc}$ and its phase was advanced by ∼90° from $I_{hrc}$. Fast Fourier transform (FFT) spectra for $I_{hrc}$ and $O_{pll}$ are shown in Fig. 8, and as shown in this figure, $O_{pll}$ oscillates at 4 kHz as $I_{hrc}$.

### 2.2. Pseudo-lock avoidance circuit

PLLs are not always locked at the howling frequency but can be locked in the harmonics of howling. Lock of the PLLs at the harmonics is generally called pseudo-lock. Fig. 9 shows an example of pseudo-lock. When we used the circuit shown in Fig. 1 with a white noise as *input*, the resulting *output* without control oscillated at ∼4 kHz. On the other hand, if we used the circuit only with the

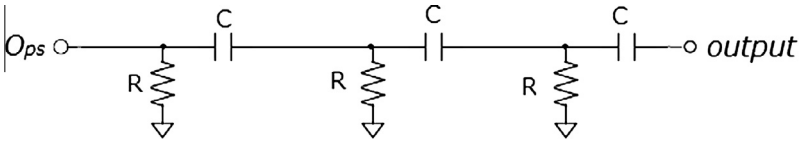


**Fig. 2.** Circuit diagram of the phase shift circuit.

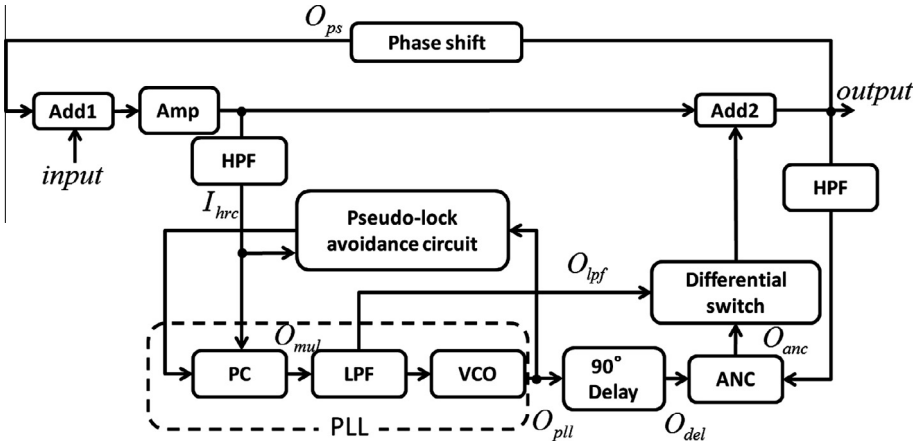


**Fig. 3.** Block diagram of howling reduction circuit.