Commun Nonlinear Sci Numer Simulat 19 (2014) 3431–3443

Contents lists available at ScienceDirect

Commun Nonlinear Sci Numer Simulat

journal homepage: www.elsevier.com/locate/cnsns

Short communication

Event-based control for memristive systems

Shiping Wen [a,b], Zhigang Zeng [a,b,*], Tingwen Huang [c]

[a] Department of Control Science and Engineering, Huazhong University of Science and Technology, Wuhan 430074, China
[b] Key Laboratory of Image Processing and Intelligent Control of Education Ministry of China, Wuhan 430074, China
[c] Texas A & M University at Qatar, Doha 5825, Qatar

ARTICLE INFO

Article history:
Received 8 April 2013
Received in revised form 9 January 2014
Accepted 2 March 2014
Available online 12 March 2014

Keywords:
Memristive system
Fuzzy model
Event-based control

ABSTRACT

This paper studies the event-based control for memristive systems. Consider the state-dependent properties of the memristor, a new fuzzy model employing parallel distributed compensation (PDC) gives a new way to linearize complicated memristive system with only two subsystems. As the existence of uncertainties of memristor and to reduce the amount of communication, event-based control algorithm to stabilize memristive systems and extend the results to systems with signal quantization and networked induced delays. Through the fuzzy modeling and distributed event-based control, there are three main advantages: (1) only two linear subsystems are considered to reduce the numbers of fuzzy rules from 2^n to $2 \times n$ as for traditional Takagi–Sugeno fuzzy model, n is the number of memristive subsystems; (2) the memristive subsystem is triggered at its own event time, which reduces communication burdens and lowers the controller updating frequency; (3) the effects of quantization and time delays are taken into account.

1. Introduction

1.1. Memristor-based circuits

As the missing fourth passive circuit element [1], memristor took scientists almost 40 years to invent it, until a team at Hewlett-Packard Labs proposed the development of a memristor in Nature on May 1, 2008 [2]. More and more attention has been attracted to the memristor because of its potential application [3–14]. The HP memristor is described as

$$v = M(q)i, \quad \text{or} \quad i = W(\varphi)v,$$

where $\varphi = \int v dt$,

$$M(q) = \frac{d\varphi(q)}{dq}, \quad \text{or} \quad W(\varphi) = \frac{dq(\varphi)}{d\varphi},$$

where $M(q)$ and $W(\varphi)$ are the memristance and memductance. Itoh and Chua assumed that the memristor is "piecewise-linear" as shown in Fig. 1. $\varphi(q), q(\varphi)$ are given by

* Corresponding author at: Department of Control Science and Engineering, Huazhong University of Science and Technology, Wuhan 430074, China. Tel.: +86 18971124190; fax: +86 27 87543130.

E-mail addresses: wenshiping226@126.com (S. Wen), zgzeng527@126.com (Z. Zeng), tingwen.huang@qatar.tamu.edu (T. Huang).

http://dx.doi.org/10.1016/j.cnsns.2014.03.004
1007-5704/

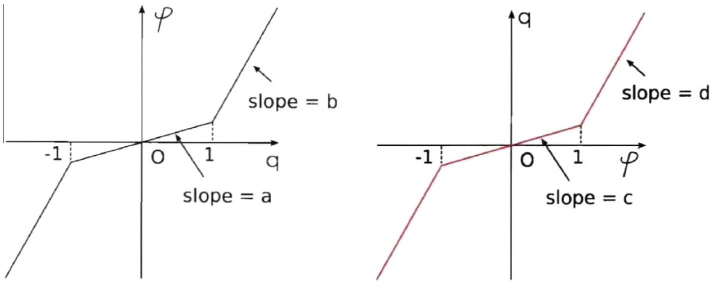

Fig. 1. The piecewise-linear memristor: Charge-controlled (left) and flux-controlled (right) memristor.

$$\varphi(q) = bq + 0.5(a-b)(|q+1| - |q-1|),$$
$$q(\varphi) = d\varphi + 0.5(c-d)(|\varphi+1| - |\varphi-1|),$$

where $a, b, c, d > 0$. memristance $M(q)$ and memductance $W(\varphi)$ are defined as

$$M(q) = \frac{d\varphi(q)}{dq} = \begin{cases} a, & |q| \le 1, \\ b, & |q| > 1, \end{cases}$$
$$W(\varphi) = \frac{dq(\varphi)}{d\varphi} = \begin{cases} c, & |\varphi| \le 1, \\ d, & |\varphi| > 1. \end{cases}$$

Consider the memristor-based Chua's circuit with a PWL memristor [6] in Fig. 2, we can get

$$\begin{cases} \frac{dV_1(t)}{dt} = \frac{1}{C_1}(i(t) - W(\varphi(t))V_1(t)), \\ \frac{dV_2(t)}{dt} = \frac{1}{C_2}(GV_2(t) - i(t)), \\ \frac{di(t)}{dt} = \frac{1}{L}(V_2(t) - V_1(t) - i(t)R), \\ \frac{d\varphi(t)}{dt} = V_1(t). \end{cases} \quad (1)$$

For technical simplicity, we set $x_1(t) = V_1(t), x_2(t) = V_2(t), x_3(t) = i(t), x_4(t) = \varphi(t)$, then

$$\begin{cases} \dot{x}_1(t) = \alpha(x_3(t) - W(x_4(t))x_1(t)), \\ \dot{x}_2(t) = \alpha_1 x_2(t) - \alpha_2 x_3(t), \\ \dot{x}_3(t) = \alpha_3(x_2(t) - x_1(t) - \alpha_4 x_3(t)), \\ \dot{x}_4(t) = x_1(t), \end{cases} \quad (2)$$

where $\alpha = \frac{1}{C_1}, \alpha_1 = \frac{G}{C_2}, \alpha_2 = \frac{1}{C_2}, \alpha_3 = \frac{1}{L}, \alpha_4 = R$,

$$W(x_4(t)) = \begin{cases} a, & |x_4(t)| \leqslant 1, \\ b, & |x_4(t)| > 1. \end{cases}$$

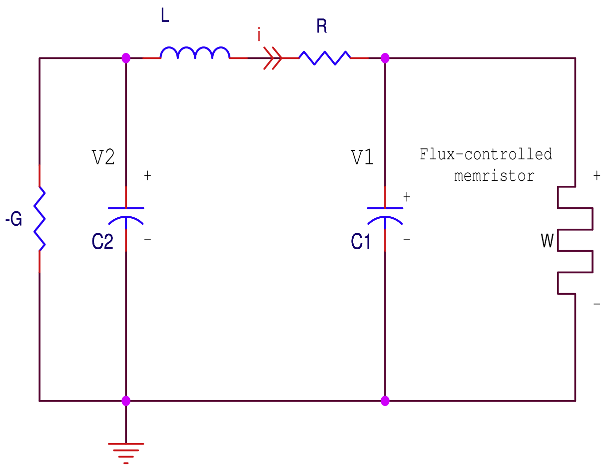

Fig. 2. Memristor-based Chua's circuit.