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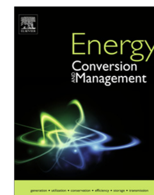

Silicon nanowire networks for multi-stage thermoelectric modules

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ABSTRACT

We present the fabrication and characterization of single, double, and quadruple stacked flexible silicon nanowire network based thermoelectric modules. From double to quadruple stacked modules, power production increased 27%, demonstrating that stacking multiple nanowire thermoelectric devices in series is a scalable method to generate power by supplying larger temperature gradient. We present a vertically scalable multi-stage thermoelectric module design using semiconducting nanowires, eliminating the need for both n-type and p-type semiconductors for modules.

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1. Introduction

Most of the energy produced commercially in the United States is lost to the environment in the form of waste heat [1]. Some of this lost energy can be recovered by mechanical heat engines via the Rankine cycle, but much of this waste heat, especially low grade (<230 °C) heat, is not considered practical to recover due to low conversion efficiencies [2]. Thermoelectric (TE) devices, which convert heat into electricity via the Seebeck effect, are an attractive option for recovering waste heat [3–5]. A range of emerging materials, expected to increase the Seebeck coefficient (S) and decrease thermal conductivity (κ), have propelled the field of TE research at the nanometer scale. While significant materials advances have been made with superlattices [6,7], nanowires [8–10], nanocomposites [11,12], thin films [13], and layered films [14], [15] there seems to be many aspects left for further advancement. In additional to material advancements the field is turning toward larger device design advancements such as p–n leg geometry [16], Fresnel lenses to intensify heat [17], as well as sandwiched traditional devices to optimize cross flow [18,19]. In this paper, by forming randomly oriented nanowire networks onto flexible metallic substrates, rather than semiconductor substrates, we build on a new concept for fabricating a TE module [20]. In this demonstration, Silicon was chosen for the TE material because of its abundance and nontoxicity. Silicon also demonstrated reduced thermal conductivity when formed into nanowires, which was beneficial to TE power generation [21–23]. Our design concept is not limited to Silicon; thus other semiconductors suitable for the desired range of temperatures, such as Indium Phosphide (InP) and Indium Antimonide (InSb) [24], which our lab has also used to demonstrate viable TE devices can be similarly implemented. As a substrate, copper was selected due to its low cost, mechanical flexibility, and high electrical and thermal conductivities. More importantly, the metallic substrate allows us to design a TE module with simple electrical connections either vertically or laterally to obtain desirable open circuit voltage (V_{oc}) and short circuit current (I_{sc}).

Conventional TE modules use a large number of small legs made of both n and p-type semiconductor to cover required device area, adding significant manufacturing costs associated with materials and assembly [25]. In these devices, V_{oc} increases as multiple p- and n-type semiconductor legs are connected in series; however, I_{sc} is limited by a narrow current path defined by the cross-sectional area of each semiconductor leg and the contact resistance associated with metal–semiconductor junctions, thus; in these devices, the series resistance increases as the number of semiconductor legs increases, limiting I_{sc} that can be achieved for a given electrical power. The concept of multi-stage TE modules presented

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in this paper offers additional unique design elements by incorporating only one type of semiconductor and a large cross sectional area as a current path into the device.

Additionally, from TE module design perspective, there is an inherent vertical scaling limitation with traditional TE modules because conventional TE modules cannot be easily stacked on top of one another to increase overall module thickness, which is partly because of heat and electrical current flowing orthogonally to each other (i.e., current flows laterally while heat flows vertically). In the multi-stage TE modules presented in this paper, heat and current flow parallel to each other, allowing for the modules to have large effective thickness that can create a large temperature gradient for a given heat source. Our approach also allows us to fabricate a TE module that is built by laterally assembling single modules made of both n-type and p-type materials, as in a conventional TE module, which is suitable for applications that require high voltage for a given power. This choice of assembling several modules allows a high current or high power module is not readily attainable with traditional TE modules.

2. Experiment

Copper (Cu) foils (approximately 50 μm thick) with area of 2 cm^2 were prepared with acetic acid, rinsed with Deionized water, and air dried. A 40 nm thick Titanium Nitride (TiN) layer was deposited onto the prepared Cu foils using an atomic layer deposition system with an inductively coupled plasma source. The TiN layer was deposited at 300 °C with N_2 carrier gas. N_2 plasma and Titanium tetrachloride, TiCl4, were utilized as the Nitrogen and Titanium precursors, respectively. Subsequently, 4 nm of gold (Au) was deposited by electron-beam evaporation onto the TiN layer.

Four samples were made for this study. All four were boron doped p-type Silicon (Si) nanowires grown in the form of three-dimensional network to promote electrical conduction while reducing thermal conductivity [26]. The Si nanowire networks were deposited by Plasma Enhanced Chemical Vapor Deposition (PECVD) with plasma generated by a 180–250 kHz 12.6 kW power source using a two-step process to form first a nanowire network and secondly a continuous semiconducting layer [27]. Precursors for the B-doped Si nanowire networks were disilane diluted in hydrogen and diborane. The PECVD process consisted of a pre-growth annealing step performed at 400 °C for 5 min in hydrogen, which was followed by a nanowire growth step at 500 °C. The disilane flow rate was 10 sccm with a reactor pressure of 0.3 Torr. The growth time for each of the four samples was different: 45, 15, 30, and 90 min for Samples 1, 2, 3, and 4, respectively. After the growth step was completed, the reaction chamber was evacuated and then the sample was cooled to 50 °C in argon.

Samples 1 and 3 were also topped with an additional p-type Si layer, referred to as "Second Si layer", which served as a top contact layer and prevented electrical and thermal shorting. This top contact Si layer was deposited by PECVD at 500 °C and 0.5 Torr for 15 min with the same precursors used for the nanowire growth. The four samples, Sample 1–4, are selectively combined to fabricate three different modules schematically shown in Fig. 1a–c. The module depicted in Fig. 1a is composed of Sample 3 and will be referred to as Module 1. The multi-stage device depicted in Fig. 1b is composed of Samples 3 and 4, referred to, from here forward, as Module 2. Samples 1, 2, 3, and 4 were used to create the device depicted in Fig. 1c and will be referred to as Module 3. The three modules, Module 1–3, were tested to obtain current–voltage characteristics, and to measure the generated electrical power output. Heat was supplied by a Joule heater to one side of the device while an active heat sink removed heat from the other side, maintaining a constant temperature gradient, regardless of different overall thickness of the three modules, at around a desired temperature. Sample 3 in each module was consistently applied to the actively cooled side of the three modules. Current–voltage measurements were made using a HP 4155A Semiconductor Parameter Analyzer parameter analyzer at a range of temperatures in the direction as heat flow, the direction normal to the Cu foil surfaces. The voltage drop measured across the stack was made with respect to the cold side as the positive terminal and the hot side as the grounded end of the stack. A 3D printed holder is utilized to hold the samples in place while ensuring good thermal contact and thermocouples are imbedded in the holders to measure the temperature at each side of the stack. The thermocouples are connected to a 24 bit national instruments thermocouple input module to a labview program to record 4 thermocouple's reading's through time.

3. Results and discussion

Scanning electron microscopy (SEM) was used to inspect characteristic growth habits of Si nanowires in Samples 1–4 as shown in Fig. 2. All four samples have nanowires with uniform high areal density and lengths exceeding 30 μm, establishing characteristic nanowire networks with a large number of interconnects. The SEM images also reveal a large variation in nanowire diameter between and within samples. Additionally, the nanowires in all samples appear to have a noticeably smooth surface. The four samples, Sample 1–4, are summarized in Table 1.

Current–voltage (*I–V*) measurements at three different temperature differentials, ~Δ0 °C, ~Δ35 °C, and ~Δ67 °C, were done on Modules 1–3 as shown in Fig. 3. All *I–V* curves are straight lines, indicating that ohmic contacts are made through the modules. The measured current for any given applied voltage increases as the temperature gradient increases, as is expected from the presence of the Seebeck effect. The slope of the *I–V* curves (i.e., conductance) for Module 1 and 2 appears to change as the average temperature changes. In Module 1, the conductance increases as the temperature gradient increases, whereas in Module 2, the conductance decreases as the temperature gradient increases. Unlike Module 1 and 2, the conductance of Module 3 remained unchanged upon increasing the average measurement temperature. The dependence of the conductance on the average measurement temperature can be explained qualitatively as follows. For semiconducting Si, the conductance is expected to increase with increasing temperature. For metallic Cu and TiN, on the other hand, the conductance is expected to decrease with increasing temperature. Therefore, the dependence of the conductance on the average measurement temperature in Fig. 3 suggests; Module 1 is dominated by the semiconducting portions, while Module 2 is dominated by the metallic portions, and, in Module 3, the conductance is equally contributed from both the semiconducting and metallic portions. The conductance of Module 3 being insensitive to the magnitude of the temperature gradient indicates that stacking multiple devices, and therefore creating additional metal–semiconductor interfaces, does not pose problems with maintaining conductance, making this architecture a vertically scalable option for building a thick TE module. The fact that the electrical conductance of Module 3 remains constant also suggests the module efficiency can be maintained through a wide range of temperatures by implementing this module architecture. The constant electrical conductance of Module 3 as the average measurement temperature increases, along with the ohmic behavior at $\Delta T = 0$, also indicates that electrical transport is not being inhibited significantly by various interfaces present in the module. As such, many nanowire networks could be stacked together, allowing for

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