Energy Conversion and Management 52 (2011) 1114–1128

Contents lists available at ScienceDirect

Energy Conversion and Management

journal homepage: www.elsevier.com/locate/enconman

Review of multilevel voltage source inverter topologies and control schemes

Ilhami Colak [a], Ersan Kabalci [b,*], Ramazan Bayindir [a]

[a] Department of Electrical Education, Faculty of Technical Education, Gazi University, Besevler, Ankara 06500, Turkey
[b] Department of Technical Programs, Vocational Collage of Haci Bektas, Nevsehir University, Hacibektas, Nevsehir 50800, Turkey

ARTICLE INFO

Article history:
Received 18 January 2010
Accepted 4 September 2010

Keywords:
Multilevel inverter
Neutral point clamped
Flying capacitor
Cascaded H-bridge
SPWM
SVM
SHE-PWM
Sigma–delta modulation
Modulation

ABSTRACT

In this study, the most common multilevel inverter topologies and control schemes have been reviewed. Multilevel inverter topologies (MLIs) are increasingly being used in medium and high power applications due to their many advantages such as low power dissipation on power switches, low harmonic contents and low electromagnetic interference (EMI) outputs. The selected switching technique to control the inverter will also have an effective role on harmonic elimination while generating the ideal output voltage. Intensive studies have been performed on carrier-based, sinusoidal, space vector and sigma delta PWM methods in open loop control of inverters. The selection of topology and control techniques may vary according to power demands of inverter. This paper and review results constitute a useful basis for matching of inverter topology and the best control scheme according to various application areas.

1. Introduction

The preliminary studies on multilevel inverters (MLI) have been performed using three-level inverter that has been proposed by Nabae. In the study, the third level has been constituted by using neutral point of DC line and the topology has been defined as diode clamped MLI (DC-MLI) [1,2]. In recent years, multilevel inverters have gained much attention in the application areas of medium voltage and high power owing to their various advantages such as lower common mode voltage, lower voltage stress on power switches, lower dv/dt ratio to supply lower harmonic contents in output voltage and current. Comparing two-level inverter topologies at the same power ratings, MLIs also have the advantages that the harmonic components of line-to-line voltages fed to load are reduced owing to its switching frequencies. The most common MLI topologies classified into three types are diode clamped MLI (DC-MLI), flying capacitor MLI (FC-MLI), and cascaded H-Bridge MLI (CHB-MLI). The hybrid and asymmetric hybrid inverter topologies have been developed according to the combination of existing MLI topologies or applying different DC bus levels respectively [3–9]. The basic topologies of MLIs are shown in Fig. 1. The recent applications of MLIs have a variety including induction machine and motor drives, active rectifiers, filters, interface of renewable energy sources, flexible AC transmission systems (FACTS), and static compensators. The diode clamped inverters, particularly the three-level structure, have a wide popularity in motor drive applications besides other multilevel inverter topologies. However, it would be a limitation of complexity and number of clamping diodes for the DC-MLIs, when the level exceeds three [10–13]. The FC-MLIs are based on balancing capacitors on phase buses and generate multilevel output voltage waveform clamped by capacitors instead of diodes. The FC-MLI topology also requires balancing capacitors per phase at a number of $(m-1)\cdot(m-2)/2$ for an m-level inverter and it will cause to increase the number of required capacitor in high level inverter topologies and complexity of considering DC-link balancing.

Among the three types of multilevel inverters, the cascade inverter has the least components for a given number of levels. Cascade multilevel inverters consists of a series of H-bridge cells to synthesize a desired voltage from several separate DC sources (SDCSs) which may be obtained from batteries or fuel cells. All these properties of cascade inverters allow using various pulse width modulation (PWM) strategies to control the inverter accurately [13–17]. In addition to these topologies, several modulation and control techniques have been developed for multilevel inverters including selective harmonic elimination PWM (SHE-PWM), sinusoidal PWM (SPWM), space vector PWM (SVM), and similar variations of the three main algorithms. The modulation methods used in multilevel inverters can be classified according to switching frequencies as seen in Fig. 2 [18–21].

The SPWM control method is very popular in industrial applications owing to its harmonic reducing opportunities by using

* Corresponding author. Tel.: +90 3844413432; fax: +90 3844413441.
E-mail address: kabalci@nevsehir.edu.tr (E. Kabalci).

0196-8904/$ - see front matter © 2010 Elsevier Ltd. All rights reserved.
doi:10.1016/j.enconman.2010.09.006

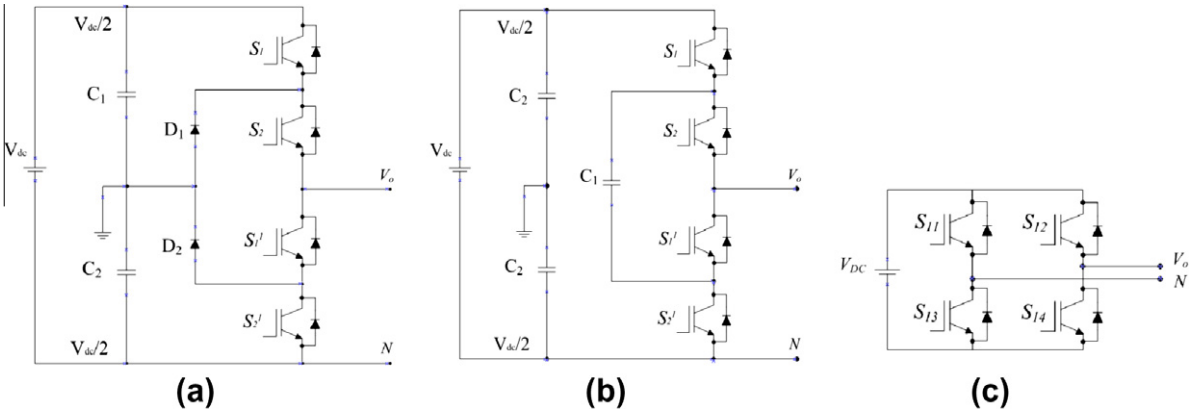

Fig. 1. Multilevel inverter topologies: (a) three-level DC-MLI, (b) three-level FC-MLI, (c) three-level CHB-MLI.

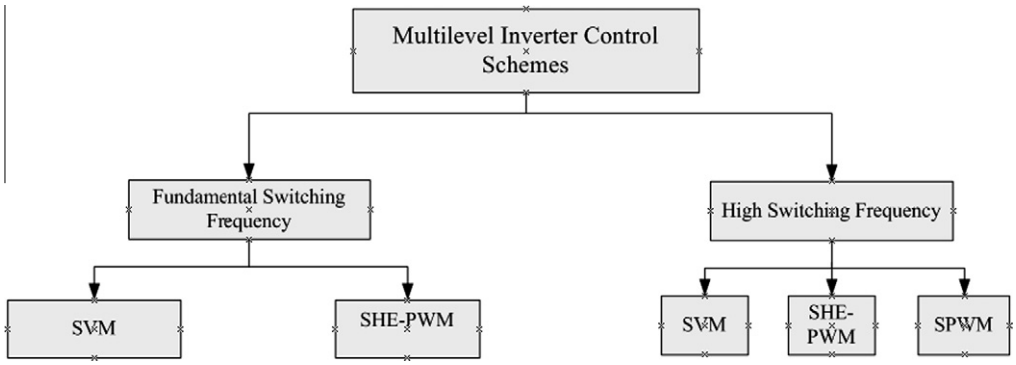

Fig. 2. Classification of multilevel inverter control schemes.

several phase shifting options on carrier signal. In the SPWM, a sinusoidal reference voltage waveform is compared with a triangular carrier waveform to generate gate signals for the switches of inverter. Several multicarrier techniques have been developed to reduce the THD ratios, based on the classical SPWM with triangular carriers. Another alternative modulation technique is SVM strategy, which has been used appropriately in three-level inverters. The SVM and SHE-PWM methods are fundamental frequency switching methods and perform one or two commutations of the power semiconductors during one cycle of the output voltages to generate a staircase waveform [22–26].

This paper presents the multilevel inverter topologies and their control methods according to existing and novel applications, based on a well-surveyed literature summary. A comprehensive study has been performed on common and hybrid multilevel inverters, and the most appropriate control schemes and applications have been proposed according to topologies.

2. Common inverter topologies

Three major multilevel inverter structures which have been mostly applied in industrial applications have been emphasized as the diode clamped, the flying capacitor, and the cascaded H-bridge inverters with separate DC sources. In addition to this, various hybrid multilevel inverters have been developed by using the three basic types mentioned above. Voltage source inverters (VSIs) are widely used in AC motor drives, AC uninterruptible power supplies (UPS), and AC power supplies with batteries, fuel cells, active harmonic filters. VSI topologies are constituted in accord with power demand of application areas and output voltages are either single phase for power demands lower than 2 kV A or three-phase for power demands over 2 kV A as being used in household and industrial loads. The semi converter, half bridge and full bridge inverters were employed for high power applications in 1990s, but recently many researchers have paid much attention to multilevel inverters for high power and medium voltage applications [27–31]. Main three multilevel inverter topologies and hybrid models of these structures have been reviewed in the following part of the paper by demonstrating sample models and control strategies.

2.1. Diode clamped multilevel inverters (DC-MLI)

The diode clamped multilevel proposed by Nabae, Takashi, and Akagi in 1981 was named as neutral point converter and was essentially a three-level diode clamped inverter as shown in Fig. 1a. Several experimental studies and articles published about results of three, four, five and six level DC-MLIs for such uses like static VAR compensators, high voltage grid interconnections, and variable speed motor drives [32–36]. A three-phase five-level DC-MLI topology is shown in Fig. 3. Each of the three-phase outputs of inverter shares a common DC bus voltage that has been divided into five levels over four DC bus capacitors. The capacitors have been subscripted from C_1 to C_4. The middle point of C_2 and C_3 capacitors constitute the neutral point of inverter and output voltages have five voltage states referring to neutral point. The voltage across each capacitor is $V_{dc}/4$ and the voltage stress on each switching device is limited to V_{dc} through the clamping diodes that have been named as $D_{1..3}$ and $D_{1..3}^{1..1}$. The key components that differ with this topology from a conventional two-level inverter are clamping diodes. To explain how the staircase voltage is synthesized, the neutral point n has been assumed as the output phase