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New cascaded multilevel inverter topology with minimum number of switches

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ABSTRACT

In this paper, a new topology of cascaded multilevel inverter using a reduced number of switches, insulated gate driver circuits and voltage standing on switches is proposed. The proposed topology results in reduction of installation area and cost and has simplicity of control system. This structure consists of series connected sub-multilevel inverters blocks. Three algorithms for determination of magnitudes of dc voltage sources have been presented, too. Validity of the analysis has been proved by simulation and experimental results.

1. Introduction

A multilevel inverter is a power electronic system that synthesizes a desired output voltage from several levels of dc voltages as inputs. Recently, multilevel power conversion technology has been developing the area of power electronics very rapidly with good potential for further developments. The most attractive applications of this technology are in the medium to high voltage ranges.

The concept of utilizing multiple small voltage levels to perform power conversion was presented by a MIT researcher [1,2]. Advantages of this multilevel approach include good power quality, good electro-magnetic compatibility, low switching losses and high voltage capability.

The first introduced topology is the series H-bridge design [1]. This was followed by the diode-clamped inverter [2–4] which utilizes a bank of series capacitors to split the dc bus voltage. The flying-capacitor (or capacitor clamped) [5] topology followed diode-clamped after few years, instead of series connected capacitors, this topology uses floating capacitors to clamp the voltage levels. Another multilevel design, slightly different from the previous one, involves parallel connection of inverter phases through interphase reactors [6]. In this design the semiconductors must block the entire voltage, but share the load current. Also, several combinatorial designs have emerged [7], implemented cascading the fundamental topologies [8–12]; they are called hybrid topologies. These designs can create power quality for a given number of semiconductor devices higher than the fundamental topologies alone due to a multiplying effect of the number of levels [13]. Also, some soft-switching methods can be implemented for different multilevel inverters to reduce the switching loss and to increase efficiency [14,15]. Recently, several multilevel inverter topologies have been developed [16–19].

Unfortunately, multilevel inverters have some disadvantages. One particular disadvantage is the great number of power semiconductor switches needed. Although low voltage rate switches can be utilized in a multilevel inverter, each switch requires a related gate driver circuits. This may cause the overall system to be more expensive and complex. So, in practical implementation, reducing the number of switches and gate driver circuits is very important.

This paper suggests a new topology for cascaded multilevel inverters with a high number of steps associated with a low number of switches and gate driver circuits for switches. In addition, for producing all levels (odd and even) at the output voltage, three procedures for calculating the required dc voltage sources are proposed. Finally, the paper includes simulation and experimental results to prove the feasibility of the proposed multilevel inverter.

2. Conventional cascaded multilevel inverters

The full-bridge topology with four switches is used to synthesize a three-level square-wave output voltage waveform. The cascaded multilevel inverter consists of series connections of n full-bridge topology. Fig. 1 shows the configuration of cascaded multilevel inverter. The overall output voltage of multilevel inverter is given by:

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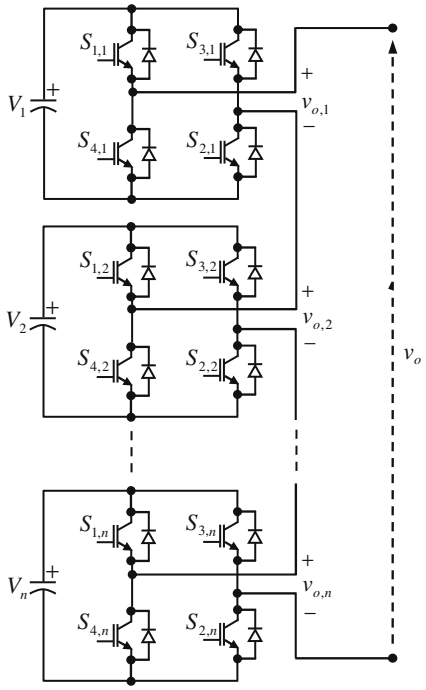

Fig. 1. Configuration of cascaded multilevel inverter.

$$v_o = v_{o,1} + v_{o,2} + \cdots + v_{o,n} \tag{1}$$

If all dc voltage sources in Fig. 1 equal to V_{dc}, the inverter is known as symmetric multilevel inverter. The effective number of output voltage steps (N_{step}) in symmetric multilevel inverter may be related to the number of full-bridges (n) by:

$$N_{step} = 2n + 1 \tag{2}$$

and the maximum output voltage ($V_{o,max}$) of this n cascaded multilevel inverter is:

$$V_{o,max} = n \times V_{dc} \tag{3}$$

To provide a large number of output steps without increasing the number of inverters, asymmetric multilevel inverters can be used. In [20,21], the dc voltages sources are proposed to be chosen according to a geometric progression with a factor of two or three. For n cascaded multilevel inverters, the number of voltage steps is given as follows:

$$N_{step} = 2^{n+1} - 1 \quad \text{if } V_j = 2^{j-1}V_{dc} \quad \text{for } j = 1, 2, \ldots, n \tag{4}$$

$$N_{step} = 3^n \quad \text{if } V_j = 3^{j-1}V_{dc} \quad \text{for } j = 1, 2, \ldots, n \tag{5}$$

The maximum output voltages of these n cascaded multilevel inverters are:

$$V_{o,max} = (2^n - 1)V_{dc} \quad \text{if } V_j = 2^{j-1}V_{dc} \quad \text{for } j = 1, 2, \ldots, n \tag{6}$$

$$V_{o,max} = \left(\frac{3^n - 1}{2}\right)V_{dc} \quad \text{if } V_j = 3^{j-1}V_{dc} \quad \text{for } j = 1, 2, \ldots, n \tag{7}$$

Comparing the Eqs. (2)–(7), it can be seen that the asymmetric multilevel inverters can generate more voltage steps and higher maximum output voltage with the same number of bridges.

3. Suggested topology

Fig. 2 shows the suggested basic unit for a sub-multilevel inverter. This consists of a capacitor (with dc voltage equal to V_{dc}) with two switches S_1 and S_2. Table 1 indicates the values of v_o for states of switches S_1 and S_2. It is clear that both switches S_1 and S_2 can not

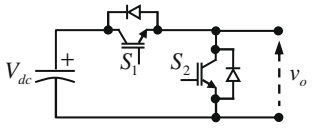

Fig. 2. Suggested basic unit for a sub-multilevel inverter.

Table 1
Values of v_o for states of switches S_1 and S_2.

State	Switches states		v_o
	S_1	S_2	
1	On	Off	V_{dc}
2	Off	On	0

be on simultaneously because a short circuit across the voltage V_{dc} would be produced. It is noted that two values can be achieved for v_o. The basic unit shown in Fig. 2 can be cascaded as shown in Fig. 3.

Although this topology requires multiple dc sources, in some systems they may be available through renewable energy sources such as photovoltaic panels or fuel cells or with energy storage devices such as capacitors or batteries. When ac voltage is already available, multiple dc sources can be generated using isolated transformers and rectifiers [22].

The overall output voltage of the suggested cascaded multilevel inverter is given by Eq. (1). Table 2 shows the values of v_o for state of switches $S_1, S_2, \ldots, S_{2n-1}, S_{2n}$. As can be seen, 2^n different values can be obtained for v_o. Fig. 4 shows a 5-level typical output

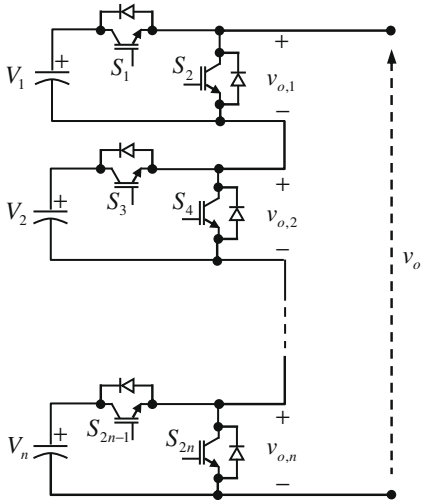

Fig. 3. Cascaded basic units.

Table 2
Values of v_o for state of switches.

State	Switches states							v_0
	S_1	S_2	S_3	S_4	$\cdots$	S_{2n-1}	S_{2n}	
1	Off	On	Off	On	$\cdots$	Off	On	0
2	On	Off	Off	On	$\cdots$	Off	On	v_1
3	Off	On	On	Off	$\cdots$	Off	On	v_2
4	On	Off	On	Off	$\cdots$	Off	On	$V_1 + V_2$
$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\cdots$	$\vdots$	$\vdots$	$\vdots$
2^n	On	Off	On	Off	$\cdots$	On	Off	$\sum_{i=1}^{n} v_1$