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Nonlinear maps from closed-loop tandems of A-to-D and D-to-A converters

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ABSTRACT

A new class of dynamical maps arises from tandems consisting of an analog-to-digital converter and a digital-to-analog converter when the latter's output is looped back to the former's input. Its nonlinear function is created when at least one of the lines between the converters is cut and that which connects to the DAC is tied to a logical High. Other maps are produced when additional DAC input lines are similarly altered, or instead clamped to a logical Low. The resulting closed-loop systems exhibit several bifurcations including that which lead to pseudo-randomness. Simulation results from numerical analysis match fairly well with those derived from an electronic circuit realization.

1. Introduction

For their possible applications in secure communications, pseudo-random number generation and cryptography, lots of researchers are drawn to the study of nonlinear maps especially to those that generate chaos: Baker [1,2], cubic [3,4], logistic [5–8], sine [9], and tent [10–13]. In this letter, the authors report about the dynamics of a new class of maps that is produced from tandems consisting of an analog-to-digital converter (ADC) and a digital-to-analog converter (DAC). It was found that several interesting transfer curves are produced when at least one of the lines connecting the two converters is cut, and the part linked to the DAC is clamped to a logical High. This simple modification results in a nonlinear relationship between the analog input and output signals so that when the output is fed back to the input, a map is created and a kaleidoscope of bifurcations may be observed as a parameter is varied. Other maps are produced when more DAC input lines are likewise altered, or instead clamped to a logical Low. In that regard, this paper reveals the results from preliminary investigations on sample members of this recently found family of dynamical maps.

The rest of the paper is organized as follows: Section 2 presents the transfer curves of some of these new nonlinearities, their mathematical representations, and the bifurcation plots describing their discrete-time dynamics as maps. In Section 3, an electronic circuit realization of one of these maps is discussed along with its bifurcation diagram. The study is concluded in Section 4.

2. Nonlinearized DAC

While the analog input and output signals from an ADC–DAC tandem are intuitively taken to be linearly related except for the effect of discretization, it is hitherto unreported that nonlinear transfer curves are produced when data lines between the

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converters are rewired. For instance, one could cut the line for the most significant bit (MSB), and the part connected to the DAC tied to a logical High. Then the next data line could likewise be severed and that part linked to the DAC tied to a logical Low as shown in Fig. 1. These two aberrations result in a nonlinear DAC (NDAC) with unique input–output characteristics.

It is immediately apparent from the foregoing that there are numerous ways to create NDACs, so it is prudent to first establish a way to distinguish one from another. For this purpose, the authors introduced the following coding scheme: For 8-bit converters, the locations of H's and L's within a byte indicate which lines are tied to logical High and Low, respectively, while the remaining unchanged lines are tagged with 1's. Based on that, HL11-1111 is the fitting label for the configuration in Fig. 1, while described in the following sections are other NDACs: LH11-1111, H111-1111, and 1H11-1111.

2.1. Transfer curve

The transfer curves of four NDACs are exhibited in Fig. 2. For each curve, BCDin stands for the ADC's binary-coded decimal (BCD) output while BCDout is equivalent to the DAC's 8-bit input as indicated in Fig. 1. If we now only consider an NDAC whose MSB line is tied to logic High, by inspection it is found that whenever bit7 of the Input byte is High, the resulting BCDout is equal to BCDin. Otherwise, BCDout is BCDin plus 2^7. In a more general sense, if the Hth data line of the DAC is tied to logical High, then

$$\text{BCDout} = \begin{cases} \text{BCDin} & (I_H = 1) \\ \text{BCDin} + 2^H & (I_H = 0) \end{cases}$$

where I_H = Hth bit of the Input byte.

It can likewise be observed that tying the DAC's Lth data line to logical Low causes a converse effect: BCDout is BCDin minus 2^L whenever the Lth bit (I_L) of the Input byte is High. Otherwise, BCDout equals BCDin. With these conditions, it is possible to further generalize the transfer functions in order to describe NDACs which have two altered lines (such as HL11-1111 and LH11-1111), with the following equation:

$$\text{BCDout} = \begin{cases} \text{BCDin} & (I_H, I_L) = (1,0) \\ \text{BCDin} + 2^H & (I_H, I_L) = (0,0) \\ \text{BCDin} + 2^H - 2^L & (I_H, I_L) = (0,1) \\ \text{BCDin} - 2^L & (I_H, I_L) = (1,1) \end{cases}$$

2.2. NDAC map

Any of the aforementioned nonlinear configurations becomes a map when its analog output (Vo) is looped back to the input (Vi) of the ADC. Moreover each map undergoes many bifurcations as a converter parameter—the Reference Voltage—is varied. For the DAC, this parameter is called VREF which when multiplied to (BCDout/256) allows one to get each of the 256 analog states. In effect, VREF sets the dynamic range of the DAC's output. Similarly the ADC uses its own reference voltage (REF+) to set the allowable range of its analog input. These elements constitute the relation between successive values of BCDout which will now be derived.

Let BCDout = g(BCDin), where $g(\cdot)$ describes the system's nonlinear transfer curve. Considering the effect of discretization, the ADC's output is given by

$$\text{BCDin} = \lfloor 2^n \text{Vi}/(\text{REF}+) \rfloor$$

where $\lfloor \cdot \rfloor$ is the floor function, n is the bit-precision of both converters, and Vi < REF+. Due to the feedback connection, Vi assumes the value of Vo = (BCDout)(VREF/2^n) hence

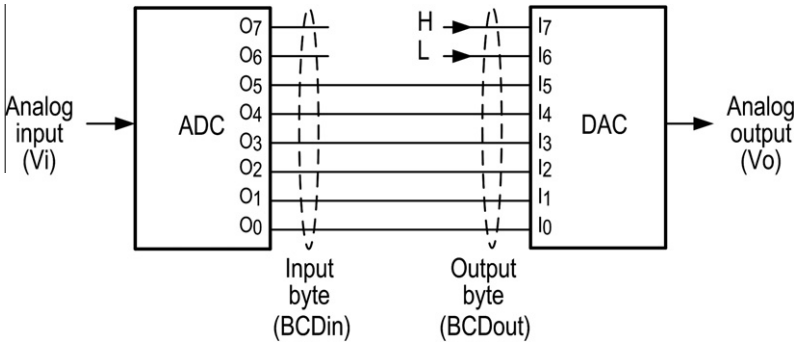

Fig. 1. ADC–DAC arrangement which produces a nonlinear transfer relationship.