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Uniform, high performance, solution processed organic thin-film transistors integrated in 1 MHz frequency ring oscillators

Simon D. Ogier[a,*], Hiroyuki Matsui[b], Linrun Feng[a], Mike Simms[a], Mohammad Mashayekhi[d], Jordi Carrabina[c], Lluís Terés[e], Shizuo Tokito[b]

[a] NeuDrive Limited, Biohub, Alderley Park, Macclesfield SK10 4TG, United Kingdom
[b] Research Center for Organic Electronics, Yamagata University, Jonan, Yonezawa, Yamagata 992-8510, Japan
[c] Universitat Autonoma de Barcelona, Escola d'Enginyeria 2ª planta, Campus UAB, 08193 Bellaterra, Barcelona, Spain
[d] Eurecat Technology Centre of Catalonia, Avenida Ernest Lluch 36, Mataro, Barcelona, Spain
[e] Institute of Microelectronics of Barcelona IMB-CNM (CSIC), Campus UAB, 08193 Bellaterra, Barcelona, Spain

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ABSTRACT

Organic electronics is one of the most promising technologies for creating flexible electronic devices using low temperature plastic compatible processes. However, contact resistances of organic transistors remain one of the most significant hurdles to achieving high performance circuits in this technology. Short channel devices (< 10 μm), essential for industrial applications, typically exhibit only a fraction of the performance promised by the high mobility results achieved in laboratory research on longer channel lengths (a few tens of μm or even longer). In this paper, we present results demonstrating solution processed devices having width-normalised contact resistances of less than 300 Ohm cm and show how these can be made into 5-stage ring oscillator circuits with the highest frequency of 1.08 MHz, corresponding to a stage delay of 93 ns. This is achieved through use of a thin, uniform high performance organic semiconductor (OSC) film made possible through formulation of a small-molecule semiconductor in a high-k binder polymer. The OSC formulation is employed in a fabrication process compatible with mass manufacture, opening up the route to commercial products made from organic thin-film transistor (OTFT) devices with high performance.

1. Introduction

Organic thin-film transistors (OTFTs) have been researched for more than 30 years and are of interest for flexible display backplane applications requiring materials that can be repeatedly bent to a small radius of curvature (< 1 mm) [1,2]. Such display applications typically incorporate photolithographically defined source-drain (S-D) electrodes of transistors with channel lengths of 5 μm or less. The charge mobility requirements for pixel transistors in this application range from below 1 cm^2/Vs for Electrophoretic (EP) and Liquid Crystal (LC) display backplanes to 5–10 cm^2/Vs or above for Organic Light Emitting Diode (OLED) display backplanes [3]. For OLED the requirement is influenced by the size and resolution of display. A significant number of organic semiconductor (OSC) materials have been reported with charge mobility exceeding 1 cm^2/Vs [4–7] but often the results are for measured OTFT devices with channel lengths of longer than 20 μm or even longer than 50 μm. An exception to this was a study reporting the short channel behaviour of dinaphtho[2,3-b:2′,3′-f]thieno[3,2-*b*]thiophene (DNTT), 2,9-diphenyl-DNTT (DPh-DNTT), 2,9-didecyl-DNTT (C10-DNTT) and pentacene [8]. They were processed in devices having channel lengths of 1 μm–100 μm and some materials demonstrated an order of magnitude reduction in apparent mobility over this range of lengths due to contact resistance effects. Such a study demonstrates a common problem with OSC materials in that it is difficult to maintain high apparent mobility in short channel devices.

Soluble OSC materials have the potential to enable low-cost electronics prototyping through the use of digital printing techniques [9]. Historically, additive printing techniques such as gravure [10] or ink-jet [11] typically exhibited low spatial resolution (> 50 μm) and had a limited capability to provide the accurate layer-to-layer registration required for transistor devices and circuits. Recent progress in this area has shown promise to meet these needs, with improved gravure printing demonstrated to better than 5 μm resolution [12–14], sub-micron scale reverse-offset printing [15] and sub-micron scale ink-jet printing [16,17] reducing the critical dimensions of printed transistor source-drain electrode gaps. Laser ablation and sintering are techniques that can be employed to fabricate 1.3 μm resolution features without the need for photomasks and have been used to create high frequency

* Corresponding author.
E-mail address: simon.ogier@neudrive.com (S.D. Ogier).

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polymer OTFTs [18]. Additionally, a combination of image analysis and digital printing has demonstrated improved layer-to-layer registration of 2 μm (3σ) on a flexible substrate through compensations for distortion [19]. Making beneficial use of the progress in micron scale printing will therefore require an improvement in the performance of OSC materials in short channel devices. Therefore, for both applications of flexible displays and high resolution printed logic devices OTFTs should have high mobility at the length scale of < 10 μm. This will enable channel length scaling to increase the frequency of operation of OTFT logic, thereby broadening the application uses of the circuits. Despite the recent progress in OSC materials, there have been only a few demonstrations of logic circuits at more than 100 kHz, far short of the theoretical frequency for such high mobility materials [20,21]. High mobility semiconductors are therefore only one of the prerequisites for fast logic circuitry and other factors must be optimised to extract the highest device performance from these materials. Short channel effects, mainly due to contact resistance, can dramatically reduce the effective mobility of the device to a fraction of the highest reported values. The cut-off frequency f_T, commonly used as a figure of merit for OTFT devices, is given by the equation [derived from equations (5) and (20) in Ref. [22]]:

$$f_T = \frac{g_m}{2\pi(C_{ch} + C_{para})} = \frac{\mu_{app} V_1}{2\pi L^2} \frac{C_{ch}}{C_{ch} + C_{para}} \quad (1)$$

where μ_{app} is the apparent mobility, L is channel length, C_{ch} is the channel capacitance, and C_{para} is the parasitic capacitance. V_1 is equal to V_D in the linear regime and to $V_G - V_{th}$ in the saturation regime, V_D is the drain voltage, V_G is the gate voltage, and V_{th} is the threshold voltage respectively. Higher frequency of operation in OTFT can therefore be achieved through decreasing channel length, reducing overlap capacitance and ensuring a high apparent mobility. The last of these can be achieved by ensuring short channel device mobility is not compromised through contact resistance effects.

In this paper we report, for the first time, organic PMOS ring oscillators with frequencies in excess of 1 MHz and stage delays of less than 100 ns. This is achieved through high mobility devices made with a 6 μm channel length having low contact resistance with the OSC layer, hence optimising two of the most important factors for increasing the cut-off frequency. The OSC formulations used are based upon the concept introduced previously, where a high mobility small-molecule and high-k polymeric semiconductor material are blended in solvent [23,24]. This approach has been shown to produce uniformly high mobility (> 4 cm^2/Vs) across a substrate by spin-coating and with good device bias stress stability. In this work we demonstrate that this formulation approach can be used to minimise contact resistance in top gate bottom contact (TGBC) OTFT devices and the effect is exemplified by using the small-molecule 1,4,8,11-tetramethyl-6,13-bis(triethylsilylethynyl)pentacene (TM-TES pentacene) [25] and high-k random copolymer 30: 70 2-[p-(diphenylamino)phenyl]-2-methylpropiononitrile: *N*,*N*-diphenyl(2,4-xylyl)amine [23].

2. Methods

2.1. Device fabrication

All fabrication was performed at the Centre for Process Innovation (CPI, Sedgefield, UK) using the Gen2 photolithography facilities (www.uk-cpi.com/pe-equipment/). OTFTs were fabricated in TGBC configuration on 8-inch square glass substrates (Corning Eagle XG) per the scheme shown in Fig. 1. Laminated plastic-on-glass substrates are compatible with the process but, due to the need to scribe the pattern accurately into several sections, a glass-only substrate was used in these trials. A planarizing layer of a proprietary acrylate polymer (PCAF, from CPI) was spin-coated, softbaked and then cross-linked using UV light in a nitrogen environment followed by hard-baking. Au source-drain electrodes (50 nm thick) were sputter coated and patterned using photolithography and wet etching. The substrates were oxygen plasma treated to increase surface energy [24] and then a self-assembled monolayer (SAM) of 3-fluoro-4-methoxythiophenol (Fluorochem, UK) was deposited from a 10 mM solution in 2-propanol by flooding the surface followed by spin-coating to dry. Subsequently two further cycles of 2-propanol deposition and spin-coating were used to rinse any excess thiol from the surface. After baking the substrate at 100 °C for 1 min, the OSC solution was spin-coated at 500 rpm for 10s followed by 1000 rpm for 60s followed by a further bake at 100 °C for 60s. The dielectric chosen for this work was Cytop CTL-809M diluted to 4.5% solids and spin-coated to give a 300 nm thick film (6 nF/cm^2 gate capacitance per unit area). The gate metal layer was thermally-evaporated gold (50 nm), patterned using photolithography and wet etching. The unwanted areas of OSC and OGI were patterned by oxygen RIE plasma etching using the gate metal as a hard-mask. A first layer of PVA based cross-linkable passivation was spin-coated and UV cross-linked. The cross-linked PVA was covered with a positive photoresist, which was patterned using photolithography, and the features in the photoresist were transferred into the PVA layer by dry etching. The remaining photoresist was then removed by UV exposure followed by development. The second passivation layer, an SU8 photopolymer, was deposited and patterned in a similar way to the PVA layer. The metal interconnect layer (50 nm Au) was sputtered and patterned using photolithography to create electrical connections where required between the metal layers. Finally, a third protective passivation layer (1 μm thick SU8 layer) was deposited and UV cross-linked followed by dry etching in a manner similar to the first two passivation layers.

2.2. Device characterisation

Single OTFT devices were measured using a Wentworth semi-auto probe station linked to a Keithley 4200 Semiconductor Characterisation System. Transfer curves were measured by applying −2 V to the drain and then scanning the gate from +30 V to −30 V with 51 data points per scan.

Contact resistances were determined from the linear regime data by calculating the channel resistance at several gate voltages and normalising them for the channel width of the transistors. The analysis was made for 3 channel lengths (22 μm, 12 μm, and 7 μm) and a line was fitted to the data to determine the intercept at zero channel length (corresponding to the contact resistance). The contact resistance was displayed as a function of gate voltage; in other cases the gate charge was calculated to compare with literature data. Ring oscillators were measured using Picoprobe 18C (input capacitance: 0.02 pF, input leakage: 10 fA) at a supply voltage of 50 V. The cut-off frequency was measured using an arbitrary function generator (AFG1022, Tektronix), a current probe (711-UHF, IST), and 2-stage amplifiers (ZFL-500-BNC, Mini-Circuits).

3. Results and discussion

3.1. Device uniformity, contact resistance and short channel effects

Devices were electrically tested after the gate layer processing and at the end of the fabrication. Table 1 shows the linear mobility values for 8 substrates tested after the gate processing; the data is displayed for each transistor channel length. Devices are of a Corbino design (see Fig. 2a inset), which eliminates parasitic source to drain current flows, hence permitting on/off ratios of in excess of 5×10^7 to be demonstrated, as can be seen by the transfer curves displayed in Fig. 2a for all the devices across the 8″ substrate. On current and linear mobility uniformity is 9% across the 8 substrates tested (n = 198 devices) demonstrating that the combination of small-molecule and high-k binder can deliver good performance over large areas despite the polycrystalline nature of the small-molecule. Linear mobility is on average