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Enhancement of the electrical performance of a printed organic thin film transistor through optimization of calendering process

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ABSTRACT

The surface roughness of a gate dielectric layer has a large effect on the electrical performance of a printed OTFT (Organic Thin Film Transistor). In this study, a treatment process called calendering is proposed to improve the electrical performance of a printed OTFT by reducing the surface roughness of the gate dielectric layer. Bottom-gate, bottom-contact structural p-type OTFT samples were fabricated by gravure printing (gate electrode and gate dielectric), inkjet printing (source/drain electrodes), and spin coating (p-type channel). Various calendering process conditions composed of temperature, speed, and nip pressure were applied in the fabrication process. Then the calendering process was optimized using the grey-based Taguchi method. For validation of the proposed method, surface roughness of the gate dielectric layer and electrical performance of the non-calendered and calendered OTFT samples were compared and analyzed. The experimental results show a significant improvement that is a 15.92% decrease in the surface roughness, a 15.46% increase in the on-off ratio, and a 30.50% increase in the field-effect mobility.

1. Introduction

Recently, various studies on organic thin film transistors (OTFT), have been conducted [1–6] with probable applications to flexible electronic devices including flexible displays. For realization of the applications, less expensive fabrication of flexible OTFT is needed. In this regard, printed electronics processes have been considered as a promising solution over conventional lithography-based processes [7,8]. Among various printing techniques for fabrication of OTFT, roll-to-roll gravure printing is more suitable in terms of cost and productivity [9,10]. However gravure printing is a type of intaglio method that transfers ink filled in intaglio patterns to substrates by contact, and so it is difficult to control the width, thickness, and smoothness in nanoscale.

OTFT composed of a gate electrode, gate dielectric, source/drain electrodes, and a channel layer functions as a switch and an amplifier. The amount of charge transfer from the source to the drain is adjusted by controlling the gate voltage. The transfer of charges that needs to be smooth to obtain a satisfactory electrical performance for commercial electronic devices is affected by multiple factors. In particular, surface roughness of the gate dielectric layer has a large effect on the charge transfer. It was reported in Ref. [11] that hills and valleys on a rough surface of the gate dielectric layer disturb charge transfer from the source to the drain, as illustrated in Fig. 1.

Because of difficulties in nanoscale control of properties in printed electronics the surface of the gate dielectric layer of a printed transistor is rougher than that of a transistor fabricated by conventional lithography-based processes. Thus, printed devices have lower electrical performance compared to ones by lithography-based processes. Therefore, many attempts have been made to improve the surface roughness of the gate dielectric layer. For example, the inkjet printing process was optimized in Ref. [12] and the surface of the printed gate dielectric layer was covered with some materials in Ref. [13]. However, they are focused on improving the surface roughness only and applicability to continuous processing has not been considered.

In this study, we propose a calendering process to improve the surface roughness of the gate dielectric layer. Calendering can reduce surface roughness by applying heat and pressure to devices using rolls. The on-off ratio and the field-effect mobility of OTFT are influenced largely by the surface roughness of the gate dielectric layer [14]. Calendering also has advantage in terms of productivity because of its compatibility with a roll-to-roll continuous process.

As for applying calendering to layers of OTFT, it was found from Ref. [14] that calendering on both the gate electrode and the gate dielectric layer showed the best improvement in the surface roughness of the gate dielectric layer and electrical performance of OTFT. But calendering factors of temperature, speed, and pressure were fixed values in the work.

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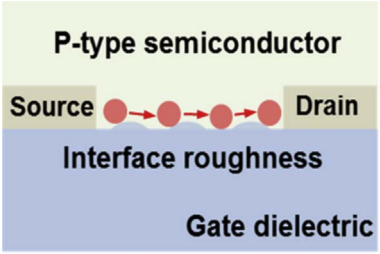

Fig. 1. Transport of charges on the rough interface of a p-type channel and dielectric layers.

This study is focused on optimization of calendering condition for OTFT. Three different levels (high, middle, and low) of the calendering factors were applied to the gate electrode and gate dielectric layer. Then the levels of the calendering factors were optimized for each layer using the grey-based Taguchi method. Finally, the surface roughness of the gate dielectric layer, the on-off ratio, and the field-effect mobility of the non-calendered and calendered OTFT samples were compared and analyzed in order to determine the effects of the calendering process.

2. Material and methods

2.1. Fabrication and measurement of OTFT samples

Bottom-gate, bottom-contact structural p-type OTFT samples, as shown in Fig. 2, were fabricated on a 0.1 mm polyethylene terephthalate (PET) substrate (SH34, SKC Ltd.) using a gravure printer, an inkjet printer, and a spin coater. First, the gate electrode was fabricated by gravure printing with a 250 cP silver nanoparticle-based conductive ink (PG-007, Paru Co. Ltd.) at 10 m/min on a PET substrate. The printed gate electrode was dried at 200 °C for 10 s using an infrared oven which is embedded in the gravure printer. For the gate dielectric layer, a 10000 cP barium titanate ($BaTiO_3$) based dielectric ink (PD-100, Paru Co. Ltd.) was used for gravure printing at 4 m/min and dried in the oven at 200 °C for 12 s. A calendering process was conducted on the gate electrode and gate dielectric layer after printing and drying. Surface roughness values of the gate dielectric layer of both the non-calendered and calendered OTFT samples were measured using an atomic force microscopy (AFM, XE-100, Park Systems Ltd.).

Since the channel length between the source and the drain needs to be shorter for better electrical performance, it was chosen to be 50 μm. Considering that the size of OTFT is a restraint for application to electronic devices, the channel width, i.e., the length of the source/drain electrodes, was designed to be 2000 μm. In addition, the width of the source and the drain was chosen as 1000 μm. See Fig. 3 for the dimensions of OTFT. Because the channel length has a large effect on the electrical performance of the OTFT, the source/drain electrodes should be printed with high accuracy. A non-contact, piezoelectric type inkjet printer (Omnijet300, Dimatix Ltd.) was used to pattern the

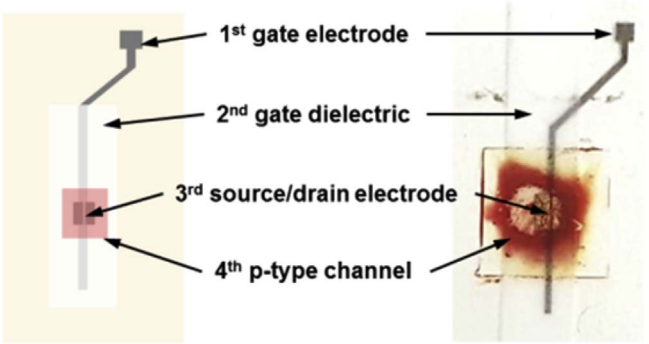

Fig. 2. Schematic and photograph of the OTFT fabricated on PET.

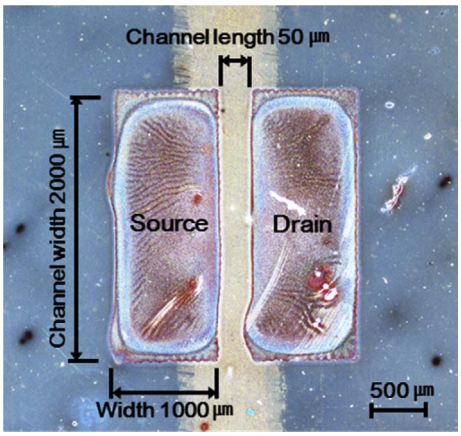

Fig. 3. Channel length and width of the OTFT.

source/drain electrodes.

The source/drain electrodes were fabricated by inkjet printing with a 14 cP silver nanoparticle-based conductive ink (PG-007, Paru Co. Ltd) and by drying at 150 °C for 5 min on a hotplate. When the source/drain electrode layer was printed, one nozzle was used with the drop space of 20 μm and the operation voltage of 25 V. A SAM (self-assembled monolayer) treatment was conducted to improve the hole transfer by reducing the Schottky barrier of the source/drain electrodes. M003 (Merck Ltd.) ink was spin coated at 500 rpm on the printed source/drain electrodes. Then it was dried on a hotplate at 100 °C for 1 min and rinsed using isopropanol. For the p-type channel, SP400 (Merck Ltd.), which is a p-type amorphous semiconductor, was spin coated at 1200 rpm on SAM-treated source/drain electrodes and dried on a hotplate at 100 °C for 4 min. A probe station (MS Tech Ltd.) and a parameter analyzer (Keithley 4200, Keithley Ltd.) were used for measuring the on-off ratio and the field-effect mobility of the printed OTFT samples. The methods and the materials used for fabrication of the OTFT samples are described in Table 1.

2.2. Calendering process

The calendering process is a finishing process for improving the surface roughness and glossiness and it has been used widely for fabric and paper substrates. This process employs a heating roll and a nip roll, as shown in Fig. 4. The surface temperature and nip pressure of the calendering process can be controlled by a heating oil system and a hydraulic system, respectively. The rotational speed can be controlled by a motor installed in the heating roll. Therefore, the calendering process is affected by three factors: temperature, speed, and pressure. During the calendering process, an OTFT sample moves between the two rolls, and temperature and pressure are applied to the surface of the sample.

In this study, three levels (high, middle, and low) of the three factors

Table 1
Materials and fabrication methods for each layer of OTFT.

Layer	Material	Ink Viscosity	Method	Curing Time	Curing Temp.
Gate electrode	Ag	250 cP	Gravure printing	10 s	200 °C
Gate dielectric	$BaTiO_3$	10000 cP	Gravure printing	12 s	200 °C
Source/drain	Ag	14 cP	Inkjet printing	5 min	150 °C
Self -assembled monolayer	M003	–	Spin coating	1 min	100 °C
P-type channel	SP400	–	Spin coating	4 min	100 °C