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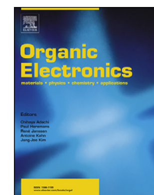

Letter

A macroscopic model for vertical graphene-organic semiconductor heterojunction field-effect transistors

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ABSTRACT

Field-effect transistors based on a graphene-organic semiconductor vertical hybrid hold great promise for applications that require a minimal driving voltage, a high current density, and a large transconductance gain. Despite impressive performances reported up to date, their working principles are still not well understood, and therefore a widely applicable functional model is now deemed essential. Here, we report on a physical current-voltage model based on the macroscopic footprints of charge transport and injection associated with the energetic asymmetry within the active diode part of a transistor. The model is composed of separate descriptions of negative and positive drain-biased circuits, which are added to build a single set of equations valid for a broad sweep range. The proposed model is validated by simulating a high-performance fullerene-based device, of which the extracted physical parameters are discussed in detail.

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Recently, triode devices incorporating a vertical heterostructure of graphene with various semiconductors have generated a great deal of interest as a novel high-performance switching component [1–6]. This unconventional device building block relies on the electric-field induced work function change of graphene [7], which in turn effectively modulates the current through the semiconductor channel, leading to an appreciable current on/off ratio (often exceeding 10^4). Among various possible channel materials, organic semiconductors may provide a particularly versatile platform, by their naturally well-matched sp^2-hybridization structure leading to the epitaxial van der Waals growth of molecular crystals on graphene surface [8–10], not to mention the well-known low-temperature large-area processability of organic materials [11].

Despite the rapidly growing technological relevance of vertical graphene-organic semiconductor field-effect transistors (VGOFETs), there is still a lack of understanding of their operation modes, and no dedicated device model has been put forward yet. Therefore, there is a timely need to develop a compact electrical description for VGOFETs that can serve as the tool for standardization of experimental observations and also as the guideline for purposeful device engineering and rational optimization [12,13].

In this letter, we present a physically based electrical model for simulation of the terminal currents of VGOFETs. The model reflects the energetic particularity of the fully depleted source-to-drain quasi-diode, in which the charge injection from the graphene contact is controlled by the gate electric field. With a reasonable number of parameters, the proposed model precisely reproduces the major characteristics of a fabricated high performance C_{60}-based transistor, and correlations are made between the circuit parameters and the governing conduction mechanisms across functional interfaces.

We start by assuming that, at zero gate voltage (V_G), the graphene source forms a blocking contact and the metal drain yields an electron-injecting contact to an n-type organic semiconductor (Fig. 1a). Here, E_b^{source} and E_b^{drain} denote the electron injection barrier from source and drain, respectively. Due to the low density of thermal carriers of an unintentionally doped organic semiconductor (ca. 10^{14} cm^{-3}), a thin organic film is assumed to be fully depleted, and therefore the metal-insulator-metal (MIM) type profiles are applicable [14,15]. This source-to-drain diode is forward biased when the drain voltage (V_D) is negative in that the applied potential gradually reduces the built-in potential (V_{bi}) across the organic layer (Fig. 1b). Initially, electrons at the drain interface diffuse toward the graphene overcoming the V_{bi}, and when the

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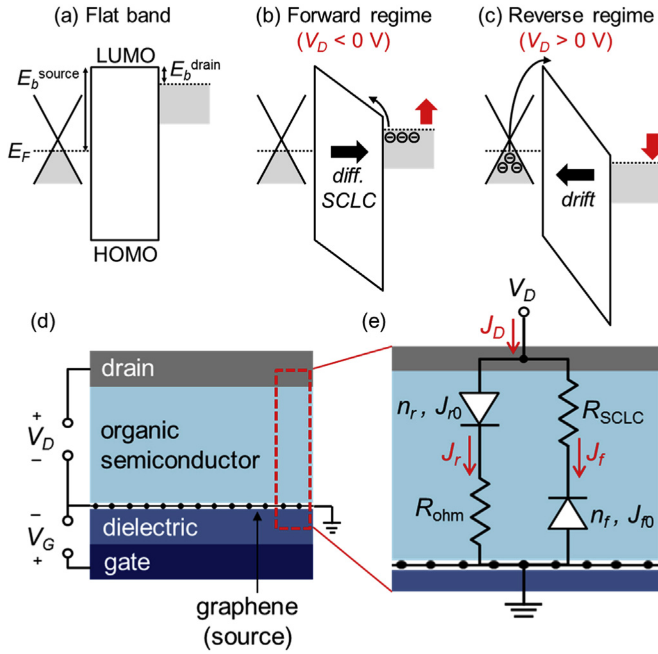

Fig. 1. (a)–(c) Energy diagram for the graphene/organic semiconductor/metal diode. The graphene contact is assumed to be p-doped and its work function is gate-controlled. In (b) and (c), the dominant carrier motion and resulting current conduction mechanisms are denoted. (d) Structure of the VGOFET. (e) Proposed electrical circuit model.

magnitude of V_D becomes larger than that of V_{bi}, the space-charge-limited conduction (SCLC) prevails as the direction of the internal electric field is inverted [15]. In contrast, Fig. 1c shows that under reverse bias ($V_D > 0$ V), the internal field always favors drift conduction of the source electrons, while their numbers are small. Note that in Fig. 1b and c, the thick arrows inside the organic layer indicate the direction of current that is opposite to the direction of electron movement.

Such a physical understanding translates into the proposed equivalent circuit model of Fig. 1e, which represents the unit area within the current-carrying two-terminal substructure out of the full device depicted in Fig. 1d. Here, the drain current density (J_D) splits into the parallel branches of the forward current density (J_f) and the reverse current density (J_r), responsible for their respective operation regimes (Fig. 1b and c). For J_f, the diffusion current is represented by a diode and the transition to the SCLC is modeled by a voltage-dependent series resistance representing the Mott-Gurney law [16–18]. Using the sign convention in Fig. 1e, we write

$$J_f = -J_{f0}\left\{\exp\left[\frac{-q\left(V_D - J_f R_{\mathrm{SCLC}}\right)}{n_f kT}\right] - 1\right\}, \tag{1}$$

with

$$R_{\mathrm{SCLC}} = -\frac{8}{9}\frac{1}{\mu\varepsilon_s}\frac{L^3}{V_D}, \tag{2}$$

where J_{f0} and n_f are the saturation current density and the ideality factor of the forward-regime diode, respectively, k is the Boltzmann constant, T is the absolute temperature, q is the elementary charge, R_{SCLC} is the area-multiplied SCLC resistance, μ and ε_s are the electron mobility and the permittivity of the semiconductor, respectively, and L is the thickness of the organic layer. For J_r, a diode accounts for the interface-related voltage drop before the linear evolution of the current, and a constant series resistance represents the drift conduction of the graphene-injected charges, yielding

$$J_r = J_{r0}\left\{\exp\left[\frac{q\left(V_D - J_f R_{\mathrm{ohm}}\right)}{n_r kT}\right] - 1\right\}, \tag{3}$$

where J_{r0} and n_r are the saturation current density and the ideality factor of the reverse-regime diode, respectively, and R_{ohm} is the area-multiplied ohmic resistance. The total current is obtained by

$$J_D = J_f + J_r. \tag{4}$$

We applied this model to a VGOFET based on graphene/C_{60} junction, first published in Ref. [4]. As shown in Fig. 2a and b, the model accurately reproduces the V_G controlled diode characteristics on both a linear and a semilog scale, with a systematically extracted set of parameters. Importantly, the rationale behind our theory also provides a clue why the maximum on/off current ratio is generally achieved on a transfer curve of a 'reverse'-biased diode (Fig. 2a inset). With increasing V_G, none of the forward-regime conduction mechanisms are considerably affected by the electron injection from graphene. Under reverse bias, on the other hand, the electron density that is exponentially dependent on the gate-controlled E_b^{source} directly affects the current level by a sharp

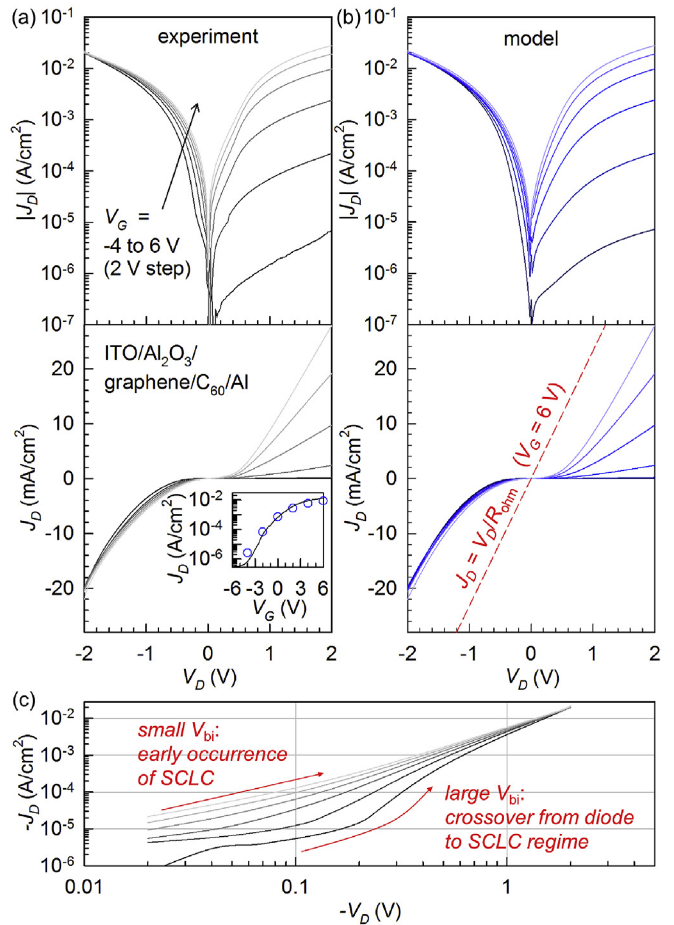

Fig. 2. (a) Measured and (b) model-reproduced output characteristics of a C_{60} VGOFET. Inset of (a) shows the measured transfer characteristic (line) as compared to the model prediction (symbol) at $V_D = 1$ V. The dashed guide line in (b) shows the slope of inverse series resistance (extracted for $V_G = 6$ V). (c) Log-log representation of the forward-regime experimental curves.

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