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Low-resistance contacts of electroless-plated metals with high-mobility organic semiconductors: Novel organic field-effect transistors with solution-processed electrodes

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ABSTRACT

The establishment of a reliable vacuum-free method for the formation of electrical contacts on high-performance organic semiconductors has become an urgent task due to rapid progress made in the development of solution-processable high-mobility organic field-effect transistors (OFETs). We have recently proposed that electroless plating, a standard technology to mass produce wirings in currently commercialized electronic devices, is suited for high-performance solution-crystallized OFETs. A low contact resistance at the source and drain electrodes is necessary with organic semiconductors for high-speed device operation; therefore, we have evaluated the contact resistance using the transfer line method. A top-contact geometry with sufficient contact area is employed to achieve stable carrier injection, which has enabled contact resistances as low as 1.4 kΩ cm on a polyethylene naphthalate substrate at a gate voltage of −10 V. This marks outstanding performance among the solution-processed metal electrodes reported for OFETs, particularly on plastic substrates. The result indicates that high-quality boundaries with minimized trap densities are realized due to the mild conditions of the electroless plating process at room temperature.

1. Introduction

Recent studies on organic devices have been aimed at lowering the production costs for electronic devices by using solution processes under ambient conditions. Organic field effect transistors (OFETs) are key devices in many digital and analog circuits, so that there is significant interest in the development of techniques to fabricate OFETs via solution processes. Recently, there has been rapid progress in the development of solution-processed organic semiconductor films [1,2]; carrier mobilities of up to 16 $cm^2 V^{-1} s^{-1}$ have been demonstrated for single-crystal OFETs fabricated by a newly developed technique where crystallized films are directly formed on substrates from solution [3]. Other reports have indicated carrier mobilities above 5 $cm^2 V^{-1} s^{-1}$ for solution-crystallized small-molecular organic semiconductors [4–6]. Such high mobilities have also been reported for polymer organic semiconductors [7,8]. These results are outstanding compared to the previous standard for solution processed bottom-contact organic transistors with typical mobilities around 1 $cm^2 V^{-1} s^{-1}$ at maximum; therefore, there is now a high expectation that printable high-performance OFETs for practical application in next-generation electronic devices, such as low-cost flexible organic integrated circuits, will be realized.

While these high-performance organic semiconductors are produced from solution under ambient conditions, the contact electrodes (source–drain electrodes) of OFETs are mostly produced by vacuum deposition [9,10]. Therefore, the next challenge in realizing low-cost printed electronic circuits is to establish a reliable vacuum-free method for the formation of electrical contacts on high-performance organic semiconductors. In line with this

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approach, we have recently demonstrated that electroless plating is feasible on solution-crystallized OFETs with carrier mobilities as high as 6 cm^2/V [11]. This is outstanding performance among reported OFETs with both semiconductor and metallic electrodes processed from solution. Inkjet processes conducted in ambient air using metal nanoparticle ink to form contact electrodes have resulted only in low mobilities of 1.2 $cm^2\ V^{-1}\ s^{-1}$ at most [12,13]. It is crucial to achieve a low contact resistance at the source and drain electrodes to operate the devices at higher speed in practical circuits; therefore, it is also essential to evaluate the contact resistance in a reliable way.

The evaluation of contact resistance requires the geometry of the OFETs to be taken into consideration, i.e., whether it features top-contact electrodes on top of the organic semiconductor or bottom-contact electrodes underneath the semiconductor layers. Top-contact devices have an advantage in that stable interfaces with low resistance can be achieved due to the large contact areas, as long as the semiconductor layers are not too thick (typically <50 nm thick films). However, this configuration bears a risk in that the patterning of the metal electrodes from solution could seriously damage the organic semiconductors during the solution process. In contrast, this risk can be avoided with bottom-contact electrodes, but with the sacrifice of smooth carrier injection at the interfaces due to the small contact area only at the edge of the electrodes. In bottom-contact OFETs, it is generally difficult to obtain a uniform crystal film because of the difference of the levels between the source–drain electrodes and channel areas; the source–drain electrodes and gate insulators are pre-fabricated on the substrate before the semiconductor layer is formed. The resulting inhomogeneity of the crystal films would thus result in poor reproducibility.

In this study, the top-contact geometry was employed to further improve the electroless plating process while minimizing the damage at the metal-to-semiconductor interfaces. Recently, our group has reported about the fabrications of fine patterning of gold source and drain electrodes on organic semiconductors using damage-less process, combining photolithography and a gold wet etching process [14]. We have adopted the same method to introduce the electroless plated contacts on organic semiconductors. The contact resistance of electroless-plated Au electrodes on a Si wafer substrate is evaluated and compared with that on a polyethylene naphthalate (PEN) substrate.

2. Contact electrodes fabricated by electroless plating

2.1. Devices with electroless-plated electrodes on a Si wafer

Firstly, a bottom-gate top-contact device with electroless-plated gold electrodes was formed on a Si wafer. An organic semiconductor layer of 3,11-didecyldinaphtho[2,3-d:2′,3′-d′]benzo[1,2-b:4,5-b′]dithiophene (C_{10}-DNBDT) was formed by vapor deposition on the surface of a 200 nm thick thermally-oxidized SiO_2 gate-insulating layer on a doped-Si substrate. The oxide surface of the gate insulator was treated with a self-assembled monolayer of n-decyltriethoxysilane using a vapor-phase epitaxial method. A 25 nm thick organic semiconductor layer was then formed by vacuum deposition through shadow masks at a deposition rate of 0.5 Å/s while the substrate was heated at 140 °C. The organic semiconductor material was synthesized by our group.

The substrate with the semiconductor layer was dipped into a 0.1% aqueous solution of trimethylstearylammonium chloride for 10 s as a pretreatment. After rinsing with deionized water, the substrate was then immersed in an Au-xylitol colloid solution (0.01%, 20 nm diameter Au nanoparticles, Electroplating Engineers of Japan, Ltd.) for 60 s. The xylitol acts as a dispersant of the Au nanoparticles. The Au nanoparticles, which act as a catalyst for electroless Au plating, were adsorbed on the organic semiconductor layer. After rinsing with deionized water, the substrate was immersed into the auto-catalytic electroless Au plating solution (PRECIOUSFAB ACG3000WX: Electroplating Engineers of Japan, Ltd.) for 300 s at 65 °C. As a result, an approximately 50 nm thick Au plating film was obtained on the organic semiconductor layer. The Au film was patterned using photolithography and gold wet etching. The fine patterning of electrodes in top-contact devices by photolithography is considered to be difficult because it seriously damages the organic semiconductor. We have recently succeeded in the fine patterning of Au electrodes on organic semiconductors by combining photolithography and a gold wet etching process [14]. The source–drain electrodes were formed by photolithography using a photoresist (OScOR2312, Orthogonal Inc.) and wet etching of the Au layer (AURUM S-50790, Kanto Chemical Co., Inc.). After each photolithography process, the photoresist films were removed using an engineered solvent (Novec™ 7100, 3M Co.).

Fig. 1 shows an optical micrograph of the fabricated device with plated contact electrodes having a channel width (W) of 2000 μm and various channel lengths (L) from 5 to 100 μm. The expanded image shows that the fine source and drain patterns are fabricated even with the channel length of 5 μm. Fig. 2 shows the FET characteristics obtained for the devices fabricated with $L = 50$ and 5 μm. The carrier mobility of the devices with the plated contact electrodes is estimated to be 1.6 and 1.0 cm^2/V for $L = 50$ and 5 μm, respectively. The carrier mobilities with the electroless-plated-contacts devices are not so deteriorated with respect to the vacuum-deposited devices for $L = 50$ μm, which we have reported previously [14]. The devices with the plated contact electrodes exhibit somewhat normally-on behavior compared to the vacuum-deposited devices. We suspect that it would be because that some residuals of the plating process have an effect to dope to organic semiconductors, and some improvements of fabrication process such as adding a cleaning process would be useful, in which details are now under study by ourselves.

The contact resistance between the organic semiconductor layer and the contact electrodes was evaluated using the transfer line method (TLM), where the drain current is measured for several devices with different channel lengths, assuming they have the same channel impedance and contact resistance. Therefore, organic semiconductor layers with a uniform mobility are preferable. Vacuum-deposited organic semiconductor layers were adopted to form uniform layers, while the Au electrodes were formed by electroless gold plating. The contact resistance R_c is defined from the following equation: $R_{tot} = R_{ch} + R_c$, where R_{tot} is the total resistance and R_{ch} is the channel resistance. Fig. 3 shows TLM plots for the devices with electroless-plated contacts at applied gate voltages from −5 to −15 V. The normalized contact resistance (R_cW) is estimated from the y-intercept of the plots to be 1.6 kΩ cm at a gate voltage (V_G) of −15 V, which is an extremely low value for an electrode fabricated under ambient conditions using a solution process. The contact resistances obtained for the electroless-plated devices are almost comparable to those fabricated by vacuum deposition on organic semiconductor films [15].

These results can be partially explained by the advantages of electroless plating, where the metal is deposited evenly on the surface of the organic semiconductor to obtain a large contact area that is favorable for low contact resistance. In inkjet processes, metal tends to aggregate in the ink, which can cause point contacts on the organic semiconductor, and thus a smaller contact area. Fig. 4 shows field emission scanning electron microscopy (FE-SEM) images of the gold plating reaction on an organic semiconductor layer. The Au films are deposited successively from the gold nanoparticles, which act as a catalyst for the plating reaction. The