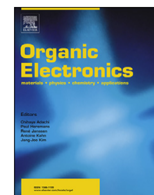
Organic Electronics 27 (2015) 155–159

Contents lists available at ScienceDirect

Organic Electronics

journal homepage: www.elsevier.com/locate/orgel



Copper phthalocyanine based vertical organic field effect transistor with naturally patterned tin intermediate grid electrode

Adan Kvitschal, Isidro Cruz-Cruz, Ivo A. Hümmelgen*

Departamento de Física, Universidade Federal do Paraná, Caixa Postal 19044, 81531-980, Curitiba, PR, Brazil

ARTICLE INFO

Article history:
Received 17 June 2015
Received in revised form
13 August 2015
Accepted 8 September 2015
Available online xxx

Keywords:
Vertical field effect transistor
Vertical organic transistor
Copper phthalocyanine
Poly(vinyl alcohol)

ABSTRACT

We report on low voltage vertical organic field effect transistors using crosslinked poly(vinyl alcohol) (cr-PVA) as gate insulator and copper phthalocyanine (CuPc) as channel semiconductor. Al is used as gate and drain electrode. Sn thin films deposited under proper conditions are used as intermediate grid electrode (source), since the Sn film morphology simultaneously shows pinholes and lateral intergrain connectivity, allowing in-plane charge transport. Our Al/cr-PVA/Sn/CuPc/Al VOFET operates at low voltages, presents specific transconductance of ~0.45 S m^{-2} and a linear source-drain current on gate voltage dependence.

© 2015 Elsevier B.V. All rights reserved.

1. Introduction

The application of organic semiconductors in planar architecture organic field-effect transistors (OFETs) [1] frequently leads to performance limitations as low output current, high operation voltage and low operational frequency. These constraints are mainly imposed by the low charge carrier mobility usually found in organic semiconductors and to particularities of the OFET channel geometry, which implies in long paths for charge carriers flowing from source to drain.

Efforts were made by several research groups to overcome these difficulties, *e. g.*, by developing organic transistors in vertical architectures [2–11], also including the use of phthalocyanines [12,13]. One of these vertical architecture devices, the Vertical Organic Field-Effect Transistor (VOFET), has a structure that provides a short channel-length path (as thick as the channel semiconductor film thickness) between the source and drain electrode and a channel with large cross section area, consequently fulfilling the basic conditions for lower operation voltages and higher output currents. In the VOFETs, gate electrode, insulator layer, intermediate electrode, semiconducting layer and top electrode are vertically stacked (see Fig. 1) and the active area *S* corresponds to the area of superposition of the electrodes. One of the key elements of these devices is the intermediate electrode that must be simultaneously permeable to the electric field and present a high enough in-plane conductivity to allow lateral connections without significant voltage drop along current paths due to in-plane film resistance. The use of an ultra-thin metallic layer deposited through evaporation is one alternative that may fulfil these requirements [14]. Additionally, Rossi et al. [7] and Seidel et al. [8] have shown that the intermediate electrode resistance can be minimized by using additional metallic or polymeric layers, respectively. There are also strategies to produce electrodes with controlled permeability like the use of sphere-lithography [15–17], co-deposition of metal and organic molecules [18], atomic layer deposition assisted nano-imprint lithography [19], random network of metallic nanowires [20], C_{60}-graphene vertical heterostructures [21] or use of block-copolymer templates [9] to obtain improved ON/OFF ratio and lower operation voltage. However, these strategies may require more complex device production steps, leading to a consequent cost rise and eliminating one of the potential advantages of the VOFETs.

In this work we report on a VOFET prepared using a Sn single layer as intermediate electrode in one-step deposition process. The use of Sn, when the optimal deposition conditions are used, simplifies the intermediate electrode preparation procedure due to the characteristics of grain growth of this material, without need of additional structuring.

* Corresponding author.
E-mail address: iah@fisica.ufpr.br (I.A. Hümmelgen).

http://dx.doi.org/10.1016/j.orgel.2015.09.010
1566-1199/© 2015 Elsevier B.V. All rights reserved.

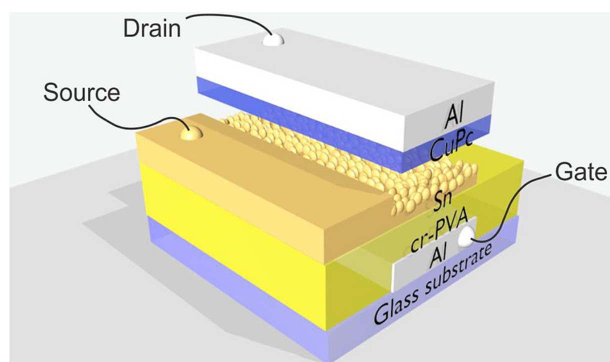


Fig. 1. Device structure of Al/cr-PVA/Sn/CuPc/Al VOFET with Sn intermediate grid electrode. The Al/CuPc layers on the top of the device are shown separately, for clarity.

2. Experimental details

The devices were prepared depositing an 80 nm thick Al electrode layer (the gate) by evaporation onto previously chemically cleaned glass substrate. In the sequence, the gate insulator was prepared depositing poly(vinyl alcohol), PVA, supplied by Sigma–Aldrich (130 kDa), used without further purification. The PVA solution was prepared as described in Ref. [22], dissolving 60 mg/mL PVA in ultrapure deionized water (resistivity > 18.2 MΩ/cm). The preparation of the cross-linked PVA (cr-PVA) films was made adding 25% w/w ammonium dichromate (AD) to the PVA solution [19]. In the sequence, an AD:PVA layer was deposited by spin coating 65 μL AD:PVA solution at 4000 rpm. The cross-linking of the PVA was achieved via 10 min UV treatment (wavelength of 365 nm, 8 W), resulting a ~350 nm thick cross-linked PVA (cr-PVA) insulating layer. The intermediate electrode (Sn) was deposited maintaining the substrate at room temperature with typical average thicknesses of 40 nm. Several evaporation rates and distances between substrate and evaporation source were tested for this step. In the sequence, we evaporated a 80 nm thick Copper Phthalocyanine (CuPc), supplied by Sigma–Aldrich and used as received. Finally, an 80 nm thick Al layer was deposited on top of the CuPc as the top electrode. The final device structure scheme can be seen in Fig. 1. The active area of the transistor, determined by the region where gate, source and drain overlap, is $S = 4\ mm^2$.

In all cases the evaporated layer geometry was controlled using shadow masks whereas material deposition was monitored using a quartz oscillator. All evaporations were made at a base pressure of 5×10^{-6} torr. Film thickness was measured with a Brucker DextakXT surface profiler. In case of the devices whose electrical characteristics are shown in the sequence the Sn evaporation rate and deposition time parameters were adjusted to obtain a resistance of 100 Ω/sq.

Transistor electrical characteristics were determined using a Keithley 2602 dual-source meter. The surface morphology was characterized by using a Shimadzu SPM-9500J3 atomic force microscope (AFM), operating in tapping mode.

3. Results and discussion

As mentioned before, one of the key elements in VOFETs is the intermediate electrode, which must be permeable to the electric field to allow affecting the channel current through the action of the gate voltage. The permeability, however, must occur without a severe increase in the in-plane resistivity of the intermediate electrode film. This condition is imposed because in a VOFET the intermediate electrode acts as injection (or in some cases as collection) electrode and must be able to transport current so efficiently as the top electrode, without suffering too high voltage drop along the film. Voltage drop would lead to an undesired position dependent potential difference between source and drain electrodes and non-uniform source-drain current density distribution. This aspect is relevant because VOFETs could be potentially applied in connection with organic light-emitting pixels where uniformity of current density and consequently of light emission in the pixel area is necessary.

The morphology of Sn thin films on cr-PVA is dependent of the particular process parameters used to obtain it (See supplementary material). For our target application, VOFETs, it is important to obtain high lateral connectivity of the grains, in order to have easy in-plane charge transport and consequently, low resistance. Both conditions were obtained placing the sample at a distance of 16 cm from the crucible at evaporation rate of 3 Å/s, with the simultaneous presence of pinholes and enough inter grain connectivity (Fig. 2). It was confirmed by a better performance in VOFETs, as will be discussed later. In case of Fig. 2(a) the deposition was stopped when the resistance of the film started to decrease, whereas in case of Fig. 2(b) the deposition was longer, stopped after the transition to low resistance occurred. Longer percolation paths of connected grains without clear border between them can be observed in case of Fig. 2(b), differently than in Fig. 2(a). But even in Fig. 2(b) free space between some of the grains (pinholes) is still observable.

It is important to mention that this was the unique investigated preparation condition which resulted devices with current modulation capability, as detailed in the sequence.

Sn thin film grown on Si as intermediate electrode was previously reported [23] in the case of permeable-base transistors (PBTs), showing high permeability to the electric field. In PBTs the permeability of a metallic layer to the electric field can be directly inferred and quantified [24]. PBTs differ from the VOFETs because injection and collection electrodes are the external ones (the base grid is the intermediate electrode, like in triode architecture) and instead of semiconductor and insulator layers as in VOFETs, PBTs use only semiconductor layers between electrodes.

The electrical characteristics of the Al/cr-PVA/Sn/CuPc/Al transistor with Sn deposited with crucible-substrate distance of 16 cm and evaporation rate of 3 Å/s (corresponding to Fig. 2) and 80 nm thick CuPc layer are shown in Fig. 3. The polarization condition (Al drain and gate are negatively biased relative to the Sn source grid) corresponds to the intermediate Sn contact acting as hole source (electron drain) and the Al top contact as hole drain (electron source). Considering the work function values of Al (4.3 eV) and Sn (~4.4 eV) [25], the highest occupied molecular orbital (HOMO) energy (~-5.2 eV) and lowest unoccupied molecular orbital (LUMO) energy (~-3.6 eV) of CuPc [26–28] and assuming absence of interface polarization, ambipolar transport through the CuPc film is in principle possible due to similar injection barrier heights for both charge carriers at both electrodes (see Fig. 3). Mobility values for both electron and holes determined in CuPc field-effect transistors are available and widely spread [29–31], the same happening with mobility values measured applying other techniques [32,33]. Phthalocyanine, however, is frequently used as hole injection or transport layer [34], in part because phthalocyanines behave as p-type material due to absorbed oxygen which acts as an acceptor level in the band gap [35]. For this reason, it is more probable that the hole transport is preponderant in our devices when the drain is negatively biased. At higher voltages, however, due to the field enhancement near to the minority carrier (electrons) injection electrode, bipolar injection is also expected to occur [36].

In Fig. 4(a) and (b) we show the drain I_{DS} and gate I_{GS} currents expressed in the corresponding current densities J for drain positively biased, respectively. As shown in Fig. 4(b), the leakage current

Download English Version:

https://daneshyari.com/en/article/7701202

Download Persian Version:

https://daneshyari.com/article/7701202

Daneshyari.com