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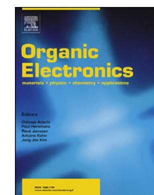

Letter

Controlled growth of a graphene charge-floating gate for organic non-volatile memory transistors

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ABSTRACT

We report memory application for graphene as a floating gate in organic thin-film transistor (OTFT) structure. For graphene floating gate, we demonstrate a simpler synthesis method to form a discrete graphene layer by controlling the growth time during a conventional CVD process. The resulting organic memory transistor with the discrete graphene charge-storage layer is evaluated. The device was demonstrated based on solution-processed tunneling dielectric layers and evaporated pentacene organic semiconductor. The resulting devices exhibited programmable memory characteristics, including threshold voltage shifts (~28 V) in the programmed/erased states when an appropriate gate voltage was applied. They also showed an estimated long data retention ability and program/erase cycles endurance more than 100 times with reliable non-volatile memory properties although operated without encapsulation and in an ambient condition.

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1. Introduction

With continued development in information technology, there is increasing interest in non-volatile memory for use as data storage in electronic devices. There are currently several types of memory devices available, which are categorized on the basis of their operating methods. Among these, a floating gate memory transistor have been widely studied owing to their non-destructive data processing, reliable data storage, and simple structure; which typically comprises a single transistor [1,2]. Those based on organic semiconductors, such as pentacene, have received particular interest by virtue of their simple process and potentials for being used as flexible or stretchable device [3]. In all floating gate memory transistors, however, the memory properties can be determined by the floating gate and tunneling dielectric. To date, conventional thin films floating gate have been used in memory transistor devices, but these conventional memory devices encounter difficulties of floating gate interference and parasitic capacitance; both of which affect the overall device performance and reliability, when used with miniaturized cell sizes and in high densities [4–9]. To overcome these problems, a number of research groups are currently searching for suitable materials that could be used to replace those used in the conventional floating gates.

Among the various potential candidates for the charge storage layer, graphene offers an advantage of introducing metallic properties [10]. Therefore, it can enhance the performance of current memory devices in a facile manner, owing to its unique properties of high density of state, high work function, and low dimensionality [11–16]. However, the two-dimensional continuous planar structure of graphene typically has difficulty in storing sufficient charge for non-volatile memory function, because the charge carrier stored in the continuous charge storage layer is easily lost through the thin tunneling dielectric. Some groups have, therefore, selected to use discrete charge storage layers, such as metal nanoparticles, for the floating gate in non-volatile memory devices [17,18].

In this study, we fabricated the graphene floating gate into the organic nonvolatile memory transistors (ONVMT) with bottom-gate/top-contact structure using pentacene and polystyrene (PS) as active and charge tunneling dielectric layers, respectively. For the floating gate, we propose a discrete graphene layer formed by controlling growth time of the graphene layer during a conventional CVD process, and then simply transferring it onto the gate

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dielectric layer. The fabricated ONVMT showed an anti-clockwise hysteresis in transfer curves with large memory windows (~40 V) and a reasonable program/erase cycle endurance greater than 100 times and an estimated long data retention time of >1 year although it was operated without encapsulation in an ambient condition.

2. Experimental procedure

In order to fabricate the partially grown graphene layer, a roll of copper foil containing 150 ppm of silver was first inserted into a quartz tube of the CVD system and then heated to 1000 °C for 40 min with flowing 40 sccm CH_2 and 5 sccm H_2 at 50 mTorr. After reaching 1000 °C, the sample was annealed for 20 min without changing the flow rate and pressure. Partially grown graphene layer was synthesized by controlling the growth time, which was varied (1, 20, 40 and 60 s) maintaining the total pressure at 100 mTorr. The CVD chamber was cooled down to room temperature with flowing only 5 sccm H_2. After the sample was taken out of the chamber, polymethylmethacrylate (PMMA) was poured on the graphene film grown on the copper foil. When floated in an aqueous solution of 0.1 M ammonium persulphate ($(NH_2)_4S_2O_8$), the PMMA with the partially grown graphene layer was separated from the copper foil [19,20].

For the memory device fabrication, a heavily doped silicon (Si) substrate with thermally grown 200 nm thick silicon dioxide insulator was used. In order to evaluate the charge storage function, two types of devices were fabricated: one with and one without the graphene floating gate. For the device with the floating gate, the partially grown graphene film was first transferred from the PMMA layer onto the SiO_2 surface and then, the charge tunneling dielectric PS was deposited from a toluene solution having the concentration of 3.5 mg/ml by spin-coating at 3000 rpm for 40 s. The film was then annealed at 120 °C for 60 min in the nitrogen atmosphere. The thickness of the obtained layer were approximately 15 nm. Finally, to deposit the active semiconductor layer and source/drain electrodes, 50 nm pentacene and 70 nm Au layers were sequentially deposited by a thermal evaporation process. The channel length and width were 50 and 1000 μm, respectively.

Atomic force microscopy (AFM) images of the graphene films were taken by using a non-contact mode of atomic force microscopy system (XE-100, Park System). Raman spectrum was measured by using Raman microsystem 2000 (Renishaw). All fabricated devices were electrically characterized in ambient and dark conditions by using a semiconductor parameter analyzer (Agilent HP 4145B).

3. Results and discussion

Fig. 1(a) illustrates schematic image of graphene growth process on Cu foil. By controlling of growth time of graphene, partially grown graphene layers with various flake size were synthesized. As shown in FE-SEM images of Fig. 1(c)–(f), graphene seed and grain grow larger with time. After 60 s (Fig. 1(f)), graphene covered all area of Cu foil with a continuous single layer. For the discrete graphene floating gate, we selected the partially grown graphene with 40 s growth time in order to ensure a large coverage of surface and guarantee discrete flake formation simultaneously. Raman spectroscopy was also used to ensure the quality of the transferred single layer graphene, the results of which are shown in Fig. 1(b). The Raman spectrum of graphene is characterized by three main characteristic peaks. The G peak, D band, and 2D peak showed at near 1580 cm^{-1}, 1350 cm^{-1}, and near 2700 cm^{-1}, respectively. The Raman spectra are measured on the edge, middle and center areas of one partially grown graphene (10×10 μm^2). The formation of monolayer graphene flakes is confirmed by a sharp 2D-band (~40 cm^{-1}) and no peak at D band (~1350 cm^{-1}).

A schematic illustration of the fabricated ONVMT is depicted in Fig. 2(a). AFM images of the evaporated pentacene and spin-coated PS layers are also shown in Fig. 2(b) and (c), respectively. The PS layer was measured to have an average thickness of ~15 nm and a root mean square roughness of 0.3 nm, which are good for an effective tunneling dielectric layer with a smooth surface for growth of the terraced pentacene film. The partially grown graphene used for the floating gate is shown in Fig. 2(d). It is noted that the graphene flake is 10 μm in the longest size and 1 nm high on average. The graphene approximately covers 80% of the total transferred area. Transmission electron micrographs (TEM) images (Fig. 2(e) and (f)) for the cross-section of the areas with and without graphene flakes in the transferred area clearly show the discrete floating gate formation.

The electrical properties of the fabricated ONVMTs are shown and compared with those of the conventional OTFTs that contain no graphene floating gate (Fig. 3). It is noted that the same structure of $p^{++}Si/SiO_2$/PS/pentacene/Au source-drain for OTFTs to compare the charge storage capability in both ONVMTs and OTFTs. Fig. 3(a) shows the transfer and output characteristics of the fabricated TFTs, which show a typical p-channel TFT behavior. Fig. 3(b) shows a double transfer curve, which obtained by sweeping gate voltage first from positive to negative values and then vice versa. Although there is a certain amount of hysteresis for the conventional OTFTs as previously reported for OTFTs with PVP gate dielectric [21–23], the hysteresis amount is very small (<5 V) in comparison with that of the ONVMTs (~40 V) when the gate voltage was swept from +80 V to −80 V and then swept back to +80 V [22]. Therefore, it can be concluded that there is almost negligible charging and discharging of the charge carriers in the bulk, or at the interfaces of the gate dielectric layer in our devices. For the fabricated OTFTs, we obtained a saturation mobility of 0.39 $cm^2/V \cdot s$, a threshold voltage of −13.2 V, a subthreshold swing of 2.6 V/decade, and an I_{on}/I_{off} ratio of ~10^6. When a graphene floating gate is inserted ($p^{++}Si/SiO_2$/graphene/PS/pentacene/Au source-drain), we obtained a larger hysteresis effect and enhanced charge storage capability. The transfer and output characteristics of the fabricated ONVMTs are illustrated in Fig. 3(c). Similar to the devices without a graphene charge layer, they exhibit typical p-channel TFT characteristics but with a saturation mobility of 0.061 cm^2/V s, a threshold voltage of −10.1 V, a subthreshold swing of 8.5 V/decade, and an I_{on}/I_{off} ratio of 10^5. It is thought that the mobility degradation is caused by the graphene floating gate and the trapped charge carriers in the graphene layer close to the pentacene surface, which introduce positive charges at the semiconductor/dielectric interface and degrade the channel conductance [17]. Fig. 3(d) shows the transfer characteristics of the fabricated ONVMTs for various sweep ranges of gate voltages (V_G), in both the forward ($+V_G$ to $-V_G$) and reverse ($-V_G$ to $+V_G$) directions, at the same drain voltage (V_D) of −20 V. This demonstrates a clear hysteresis loop for all gate voltages and for the range of +80 V to −80 V, the resulting memory window was 40 V. This confirms that the charges were successfully transferred between the pentacene and the graphene layers. Moreover, the anticlockwise hysteresis direction indicates that electrons were injected from the pentacene to graphene layer when a positive gate bias was applied, and ejected from the graphene to pentacene layer when a negative gate bias was applied [24].

To evaluate the programming and erasing properties, the shift in the transfer curves from the initial state was measured after applying a gate voltage of +80 V and −80 V, respectively, for 100 ms. The drain-source voltage was kept constant at −20 V in both measurements. Fig. 4(a) shows the programming and erasing characteristics of the ONVMT, in which large V_{th} shifts are shown.

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