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Optimizing pentacene thin-film transistor performance: Temperature and surface condition induced layer growth modification

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ABSTRACT

In this work we present *in situ* electrical and surface analytical, as well as *ex situ* atomic force microscopy (AFM) studies on temperature and surface condition induced pentacene layer growth modifications, leading to the selection of optimized deposition conditions and entailing performance improvements. We prepared p^{++}-silicon/silicon dioxide bottom-gate, gold bottom-contact transistor samples and evaluated the pentacene layer growth for three different surface conditions (sputtered, sputtered + carbon and unsputtered + carbon) at sample temperatures during deposition of 200 K, 300 K and 350 K. The AFM investigations focused on the gold contacts, the silicon dioxide channel region and the highly critical transition area. Evaluations of coverage dependent saturation mobilities, threshold voltages and corresponding AFM analysis were able to confirm that the first 3–4 full monolayers contribute to the majority of charge transport within the channel region. At high temperatures and on sputtered surfaces uniform layer formation in the contact–channel transition area is limited by dewetting, leading to the formation of trenches and the partial development of double layer islands within the channel region instead of full wetting layers. By combining the advantages of an initial high temperature deposition (well-ordered islands in the channel) and a subsequent low temperature deposition (continuous film formation for low contact resistance) we were able to prepare very thin (8 ML) pentacene transistors of comparably high mobility.

1. Introduction

Organic electronics, the extensive field of employing the electronic properties found in polymers and small organic molecules, is already far beyond being a primarily research specific term. It is frequently used in today's marketing strategies for electronic devices, symbolizing high quality, cutting-edge technology [1,2]. The organic systems inherent advantage of room temperature processing and patterning, enables a completely new class of temperature critical substrates and materials, with associated qualities such as low-cost, flexibility and bio-degradability [3,4]. With the first systems achieving commercial status, scientific focus expands from the hands-on creation of organic thin film transistor (OTFT) devices towards more and more fundamental research. Indeed, device features of critical interest, such as transistor performance and organic semiconductor growth, are to the present date not fully understood and controllable in satisfactory detail [5–8].

Being part of organic field effect transistor research and development for almost 25 years [9,10], the polycyclic aromatic hydrocarbon pentacene ($C_{22}H_{14}$) has earned its reputation as a working horse material in OTFT fabrication. This is for the most part attributable to the attainable high charge carrier mobilities and can be related to the materials tendency to form well-ordered layers of standing molecules with excellent long axis alignment of the five linearly connected benzene rings, which form the molecules structure [11]. To gain conclusive insight into thin-film growth and the connected electrical properties recently several groups turned their attention to *in situ* measurements under vacuum conditions, in an effort to improve reproducibility and reduce atmosphere induced contamination and degradation [12–20]. These groups were able to show that ultra-high vacuum (UHV) chamber deposition in combination with *in situ* surface analytical and electrical characterization methods are able to accurately connect active layer growth and morphology with the resulting electrical transistor properties, based on specific, well-controlled surface alterations [21,22].

One distinguished point of interest is the number of closed monolayers (ML) at which the rise in mobility with increasing

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coverage saturates and therefore indicates the maximum effective Debye length in the film [23,24]. This was subject-matter of a number of articles [14,15,19,20,23–27] and was also discussed to some extent in our previous publication [28]. In this work we reported a saturation of the mobility at a layer thickness of about 4 monolayers (approximately 6.4 nm) for low temperature (200 K) layers. For room temperature deposition a significant additional mobility increase up to 50 nm layer thickness was observed. This was attributed to a decrease of the access resistance due to better, continuous film formation in the silicon dioxide–gold electrode transition region [28].

The complementary measurements described in this contribution address and expand the aforementioned reports for pentacene growth. Pentacene layers have been deposited on carbon contaminated as well as sputter cleaned SiO_2 for sample temperatures up to 350 K. This allowed us to gain further insight into the optimal processing temperatures for pentacene deposition for a range of semiconductor thicknesses. Based on the gained information we were able to prepare mixed layer systems, featuring different sample temperatures during deposition, which showed improved transistor behavior.

2. Experimental

2.1. Film preparation and surface analytical characterization

Our experimental setup enables full control over the semiconductor deposition process through precise deposition temperature and rate adjustment, as well as exact sample surface temperature control and variation between 120 K and 800 K, during and subsequent to the deposition itself. The sample surface and deposited layers can be modified by argon ion sputtering and analyzed by Auger electron spectroscopy (AES) as well as thermal desorption spectroscopy (TDS). Electrical characterization was performed via a self-designed LabVIEW® processing software. *Ex situ* AFM was used to characterize the morphology of the films. A detailed description of the sample preparation, vacuum equipment and experimental methods at our disposal can be found in our previous publication [28].

2.2. Electrical characterization

While not always applicable to its full extent [23,29], the formalism developed for silicon based field effect transistors has proven to be the most efficient and intuitive way to compare the performance characteristics between samples and with results from other research groups. By setting either the drain-source voltage (U_{DS}) and sweeping the gate-source voltage (U_{GS}) or vice versa and measuring the resulting source-drain current (I_{DS}), transfer and output characteristics can be generated, which in turn contain the necessary information to extract the parameters of relevance for organic transistor characterization, in our case the charge carrier mobility (μ) and the threshold voltage (U_T) [30]. For our investigations the saturation mobility (μ_{Sat}) as a function of coverage was the main point of interest, extracted from the well-known formula:

$$I_{DSSat} = C_G \mu_{Sat} \frac{W}{2L} [U_{GS} - U_T]^2 \text{ for } |U_{DS}| > |U_{GS} - U_T| > 0 \quad \text{(saturation regime)} \tag{1}$$

with the aforementioned parameters for the saturation condition, as well as the gate capacitance of SiO_2 C_G (23 nF/cm^2), the channel width W (4 mm) and length L (25 μm) [28].

2.3. Preparation condition matrix

The main intention of this work was to reach a comprehensive understanding of the influence of film preparation parameters on the transistor properties. For this purpose, we deposited pentacene films on a SiO_2 bottom-gate, gold bottom-contact configuration at three different temperatures (200 K, 300 K, 350 K). Following our preceding investigations [28] on substrates, which had been sputter cleaned before creating a carbon saturation layer (labeled as Sputtered + C), we expanded our investigations to the contrasting surface conditions of unsputtered and subsequently carbon covered (labeled Unsputtered + C) as well as sputter cleaned samples (labeled Sputtered). The carbon saturation layer was established by repeated adsorption/desorption cycles of pentacene layers, as described in more detail in our previous paper [28]. For all of the samples (3 temperatures, 3 surface conditions) we have performed full *in situ* electrical characterization via output and transfer curves and subsequently investigated the film morphology by *ex situ* AFM in the SiO_2 channel region, the gold contact region and in the very important SiO_2–Au transition region. This resulted in a ($3 \times 3 \times 3$) information matrix. Additionally, our systems unique possibility of repeated pentacene deposition and removal allowed us to perform the depicted coverage dependency measurements on a single silicon wafer sample for each parameter set and therefore ensured optimal reproducibility for the displayed results. The obtained values for the mobilities and threshold voltages showed excellent agreement with our previous measurements for similar parameter sets. This comparability of measurements performed over a timespan of more than a year and over 50 samples is proof of the reliability and reproducibility provided by our experimental setup.

3. Results and discussion

3.1. Coverage dependent mobility on Unsputtered + C samples

A series of pentacene transistors have been prepared on the Unsputtered + C sample surface at 200 K, 300 K and 350 K. The corresponding output and transfer curves have been recorded for parameter extraction, in particular the mobility and threshold voltage as a function of coverage. Characteristic output and transfer curves for the three temperature regimes are shown in Figs. 1–3. The non-linearity for low drain-source voltages (U_{DS}) in Figs. 2 and 3 can be related to contact resistance effects [30]. The mobility evolution with increasing pentacene layer thickness for these temperatures in a coverage range of 0–150 nm, as well as an inset depicting the formation of the first percolation layer for electrical conductivity at low coverage are shown in Fig. 4.

3.1.1. Pentacene deposition at 200 K and 300 K

An immediately observable feature in the electrical evaluations is the excellent reproducibility within error margins when it comes to the extracted mobility values for the two 300 K measurements on the Unsputtered + C surface. The first source-drain currents and therefore mobilities larger than zero can be observed at around 1.2–1.5 nm nominal pentacene coverage for the 200 K and 300 K layers (see inset in Fig. 4), equivalent to a layer thickness of approximately 0.75 monolayers, which in turn shows good agreement with the postulated percolation threshold of about 0.7 monolayers reported by other groups [31–33]. The maximum recorded saturation mobilities for both temperatures on the Unsputtered + C surface are roughly a factor of 10 lower than the previously published results on the Sputtered + C samples [28], indicating a strong influence of the surface preparation. The 200 K growth shows mobility saturation at the completion of 3–4 monolayers, corresponding to approximately 5–7 nm of nominal pentacene