ELSEVIER

Contents lists available at ScienceDirect

## **Organic Electronics**

journal homepage: www.elsevier.com/locate/orgel



# Low voltage and time constant organic synapse-transistor



Simon Desbief<sup>a</sup>, Adrica Kyndiah <sup>b,c</sup>, David Guérin<sup>a</sup>, Denis Gentili<sup>b</sup>, Mauro Murgia<sup>b</sup>, Stéphane Lenfant<sup>a</sup>, Fabien Alibart<sup>a</sup>, Tobias Cramer <sup>b,e</sup>, Fabio Biscarini<sup>d</sup>, Dominique Vuillaume <sup>a,\*</sup>

- a Institute for Electronics Microelectronics and Nanotechnology, CNRS and University of Lille, Av. Poincaré, F-59652cedex, Villeneuve d'Ascq, France
- <sup>b</sup> Consiglio Nazionale delle Ricerche, Istituto per lo Studio dei Materiali Nanostrutturati (CNR-ISMN), Via P. Gobetti 101, 40129 Bologna, Italy
- <sup>c</sup>Alma Mater Studiorum-Università degli Studi di Bologna, Dipartimento di Chimica "G. Ciamician", Via Selmi 2, 40127 Bologna, Italy
- <sup>d</sup> Life Science Dept., Univ. Modena and Reggio Emilia, Via Campi 183, 41125 Modena, Italy
- e Università di Bologna, Dipartimento di Fisica e Astronomia, Viale Berti Pichat 6/2, Bologna, Italy

#### ARTICLE INFO

# Article history: Received 7 December 2014 Received in revised form 17 February 2015 Accepted 18 February 2015 Available online 24 February 2015

Keywords: Organic synapse Nanoparticle Memory Memristor Transistor

#### ABSTRACT

We report on an artificial synapse, an organic synapse-transistor (synapstor) working at 1 V and with a typical response time in the range 100–200 ms. This device (also called NOMFET, Nanoparticle Organic Memory Field Effect Transistor) combines a memory and a transistor effect in a single device. We demonstrate that short-term plasticity (STP), a typical synaptic behavior, is observed when stimulating the device with input spikes of 1 V. Both significant facilitating and depressing behaviors of this artificial synapse are observed with a relative amplitude of about 50% and a dynamic response <200 ms. From a series of *in-situ* experiments, i.e. measuring the current–voltage characteristic curves *in-situ* and in real time, during the growth of the pentacene over a network of gold nanoparticles, we elucidate these results by analyzing the relationship between the organic film morphology and the transport properties. This synapstor works at a low energy of about 2 nJ/spike. We discuss the implications of these results for the development of neuro-inspired computing architectures and interfacing with biological neurons.

© 2015 Elsevier B.V. All rights reserved.

#### 1. Introduction

There is a growing interest in neuro-inspired devices based on emerging technologies beyond the existing silicon CMOS implementation of artificial neural networks (e.g. see recent reviews in a special issue [1] and in Refs. [2,3]). Organic bioelectronics is emerging as a viable technological approach aiming at interfacing organic devices with cells and neurons [4–6]. We have recently demonstrated how we can use charge trapping/detrapping in an array of gold nanoparticles (NPs) at the SiO<sub>2</sub>/pentacene interface to design a synapse-transistor (synapstor) mimicking the dynamic plasticity of a biological synapse [7,8]. This device called NOMFET (Nanoparticle Organic Memory Field Effect Transistor) combines a memory and a transistor effect in a single device. NOM-FETs have been initially designed for neuro-inspired computing architectures (artificial neural networks). This device (which is memristor-like) [8] mimics short-term plasticity (STP) [7] and temporal correlation plasticity (STDP, spike-timing dependent plasticity) [8] of biological spiking synapses, two "functions" at the basis of learning processes. A compact model was developed

E-mail address: dominique.vuillaume@iemn.univ-lille1.fr (D. Vuillaume).

[9] and we demonstrated an associative memory, which can be trained to exhibit a Pavlovian response [10]. However, these devices were limited to work with spikes in the range of few tens of volts and time scale of 1–100 s. Both fields (neuro-inspired computing and bioelectronics) require devices working at lower voltages (to save energy consumption during computing and because action potentials in synapse and neurons have amplitudes of around 100 mV) and higher speed (e.g. synapse and neurons work at around kHz).

Here, we report on a synapstor working at 1 V and with a typical response time constant in the range 100-200 ms. To gain a better insight of the NOMFET behavior, we performed a series of *in-situ* experiments where the response of the device is studied during the growth of the organic semiconductor thin film. We analyzed the relationship between the organic film morphology and the transport properties by measuring the current–voltage characteristic curves, *in-situ* and in real time, during the growth of the pentacene over the NP network. Second, we performed temperature-dependent measurements of the charge carrier mobility to assess the effect of NPs on charge transport properties. Finally, based on the conclusions drawn from these experiments, we report on an optimized NOMFET fabrication process getting a larger hole mobility of the NOMFET ( $\sim 0.1 \text{ cm}^2/\text{Vs}$ , instead of  $10^{-3} - 10^{-2} \text{ cm}^2/\text{Vs}$ 

<sup>\*</sup> Corresponding author.

in our previous work) [7] and a faster response time constant (hundreds of ms instead of few seconds).

#### 2. Materials and methods

#### 2.1. Si/SiO<sub>2</sub> wafer substrate and source/drain electrodes

The NOMFETs were processed using a bottom-gate electrode configuration. We used highly-doped (resistivity  $<10^{-3} \Omega$  cm) ntype silicon covered with a thermally grown 200 nm thick silicon dioxide (grown at 1100 °C during 135 min in a dry oxygen flow (2 L/min) and followed by a post-oxidation annealing at 900 °C during 30 min under a nitrogen flow (2 L/min) in order to reduce the presence of defects into the oxide). Electrodes (titanium/gold (20/200 nm)) were deposited on the substrate by vacuum evaporation and patterned by e-beam lithography for linear source and drain gold electrodes (length  $L = 1-50 \,\mu\text{m}$  and width  $W = 1000 \mu m$ ) and by optical lithography for interdigitated source and drain gold electrodes (length L = 20 and  $40 \,\mu\text{m}$ , width W = 11,200 and 22,400 µm). Before use, these wafers were cleaned following the protocol: (i) sonication in acetone for 15 min and isopropanol (15 min), dried in  $N_2$ , (ii) piranha solution ( $H_2SO_4/H_2O_2$ , 2/1 v/v) for 15 min (Caution: preparation of the piranha solution is highly exothermic and reacts violently with organics), (iii) rinse with DI water, copiously, (iv) etch with HF 2% for 5 s, rinse with DI water, copiously, dry in N2 and bake at 120° (hot plate), or clean by ultraviolet irradiation in an ozone atmosphere (ozonolysis) for 30 min. The cleaned substrates are used immediately (see surface functionalization below).

#### 2.2. Au NPs synthesis

Colloidal solutions of citrate-capped Au NP (10 ± 3 nm in diameter) were synthesis as follows [11]. Charge stabilized Au nanoparticles were synthesized by the reduction of chloroauric acid in water. To obtain a 100 mL aqueous solution of Au nanoparticles, a solution with 1 mL of HAuCl<sub>4</sub>4H<sub>2</sub>O (1% w/v) in 79 mL of H<sub>2</sub>O was first prepared. A 20 mL reducing solution with 4 mL of trisodium citrate (1% w/v) and 80  $\mu$ L of tannic acid (1% w/v) in 16 mL of H<sub>2</sub>O was then added rapidly to the Au solution (all solutions at 60 °C). The mixed solution was boiled for 10 min before being cooled down to room temperature. A continuous stirring was applied throughout the process. The resulting reddish solution contained typically 10 nm Au. The NP size (10 ± 3 nm in diameter) and density is calculated from SEM images of NPs arrays on the surface (as the one in Fig. S1 in SI).

#### 2.3. SiO<sub>2</sub> surface functionalization and NP deposition

Immediately after the cleaning (see above), the SiO<sub>2</sub> gate dielectric was functionalized by self-assembled monolayer (SAM) to anchor gold nanoparticles (NPs) on the surface [12]. The SiO<sub>2</sub> surface was functionalized by immersion in a solution of (3-aminopropyl)-trimethoxysilane (APTMS) molecules diluted in methanol at a concentration  $1 \mu L/mL$  for 1 h [13]. The reaction took place in a glove-box with a controlled atmosphere (nitrogen, with less than 1 ppm of oxygen and water vapor). Excess, non-reacted, molecules were removed by rinse in methanol under sonication. This sample was subsequently dried under nitrogen stream. Static water contact angle was 19°, a common value for hydrophilic NH<sub>2</sub>-terminated surfaces [13]. This sample was then immediately dipped in a colloidal solution of citrate-stabilized Au-NP for 24 h. This procedure yields an array of NPs with a density of about 4- $5 \times 10^{10} \, \text{NP/cm}^2$  (see details in the Supporting Information, Fig. S1). The sample was then cleaned with deionized water and isopropanol, and dried under nitrogen stream. The NPs deposited on  $SiO_2$  do not form a continuous film or large clusters, rather they are adsorbed as individual entities. They do not coalesce (mainly due to coulombic repulsion between the negatively charged citrate layer), and they exhibit a characteristic length scales, i.e. a density, that we can adjust with the concentration of the Au NPs in the solution and the time of deposition [7]. Indeed, we have previously demonstrated that an optimized density of NPs for the NOMFETs is around  $5 \times 10^{10}$  NP/cm<sup>2</sup> [7].

#### 2.4. OTS functionalization

Octadecyltricholorosilane (OTS) molecules were used as follow [14,15]. The silanization reaction was carried out in a glovebox under nitrogen atmosphere but non-anhydrous solvents were used to favor hydrolysis of  $-\text{SiCl}_3$  functions. The freshly cleaned substrate was immersed for 2 h in a  $10^{-3}$  M solution of OTS in a mixture of n-hexane and dichloromethane (70:30 v/v). The device was rinsed thoroughly by sonication in dichloromethane (2 times) then blown with dry nitrogen.

#### 2.5. Pentacene evaporation

For *in-situ* experiments. Pentacene was evaporated at a rate of 0.5 ML/min ( $\sim$ 0.125 Å/s, 1 ML of pentacene  $\approx$ 15 Å). The substrate was kept at room temperature. About 20 ML (30 nm) were evaporated. For device measurements (*ex-situ*), a 35 nm thick pentacene film was evaporated at a rate of 0.1 Å/s. The substrate was kept at 60 °C. 4 devices were fabricated in parallel during the same pentacene evaporation run: (i) a reference pentacene transistor without NPs (and without APTMS SAM on SiO<sub>2</sub>) – referred to as P5, (ii) a second pentacene transistor with an OTS functionalized SiO<sub>2</sub> gate dielectric – referred to as OTS-P5, (iii) a "standard" NOM-FET, with APTMS and NPs – referred to as APTMS-NP-P5, (iv) the "optimized" NOMFET with the OTS treatment and referred to as APTMS-NP-OTS-P5.

#### 2.6. AFM measurements

The surface morphology of the organic layer was determined by imaging with a Bruker ICON atomic force microscope (AFM) in tapping mode. Silicon cantilevers from Bruker (NCHV model) were used to acquire AFM images of  $5\times 5~\mu m^2$  at 1 Hz with a resolution of  $512\times 512$  pixels.

#### 2.7. Contact angle measurements

The wettability of the surface at different stages of the fabrication was assessed by measuring the water contact angle. We measured the static water contact angle with a remote-computer controlled goniometer system (DIGIDROP by GBX, France). We deposited a drop (10–30  $\mu L)$  of deionized water (18  $M\Omega~cm^{-1})$  on the surface, and the projected image was acquired and stored by the computer. Contact angles were extracted by contrast contour image analysis software. These angles were determined a few seconds after application of the drop. These measurements were carried out in a clean room (ISO 6) where the relative humidity (50%) and the temperature (22 °C) are controlled. The precision with these measurements are  $\pm 2^{\circ}$ .

#### 2.8. Electrical measurements

For *in-situ* measurements, just before pentacene evaporation, samples were transferred in the home-built vacuum evaporation chamber [16], the bottom gate and the bottom source/drain electrodes were electrically connected, and drain current-gate voltage

### Download English Version:

# https://daneshyari.com/en/article/7701687

Download Persian Version:

https://daneshyari.com/article/7701687

<u>Daneshyari.com</u>