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Realization of electrically stable organic field-effect transistors using simple polymer blended dielectrics

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ABSTRACT

Organic field-effect transistors (OFETs) were fabricated using polymer blended gate dielectrics in an effort to enhance the electrical stability against a gate bias stress. A poly(melamine-co-formaldehyde) acrylated (PMFA) gate dielectric layer with great insulating properties was blended with polypentafluorostyrene (PFS), a type of hydrophobic fluorinated polymer. Although the overall electrical performance dropped slightly due to the rough and hydrophobic surfaces of the blend films, at the blend ratio (10%), the OFET's threshold voltage shift under a sustained gate bias stress applied over 3 h decreased remarkably compared with an OFET based on a PMFA dielectric alone. This behavior was attributed to the presence of the hydrophobic and electrically stable PFS polymer, which provided a low interfacial trap density between the gate dielectric and the semiconductor. A stretched exponential function model suggested that the energetic barrier to create trap states was high, and the distribution of energetic barrier heights was narrow in devices prepared with PFS.

1. Introduction

Organic blends are widely used to fabricate organic field effect transistors (OFETs), which show tremendous promise as flexible, low-cost, large-area electronic devices [1–3]. The organic blend strategies have been used to simplify the processing steps and to take advantage of the complementary properties of two or more organic materials present in a single solution. Previous studies of organic blend-based OFETs may be classified into three categories of blends: semiconductor/dielectric, dielectric/dielectric, and semiconductor/semiconductor blends. Recently, several research groups have investigated the use of semiconductor/dielectric blends in forming vertically phase-separated structures during the solution processing step. These structures formed due to the large difference between the surface energies of the two materials. The hydrophobic semiconductor moved toward the air/film interface and the hydrophilic dielectric materials moved toward the substrate/film interface. The graded structure yielded an OFET with a typical bottom-gate, top-contact structure that displayed hysteresis-free device operation and high field-effect mobilities (μ_{FET}s) [4]. Similarly, our group has described the preparation of a vertically phase-separated structure in a dielectric/dielectric blend to obtain high-performance p- and n-type OFETs [5]. Hydrophilic poly(melamine-co-formaldehyde) acrylated (PMFA), which has excellent insulating properties, was mixed with a hydrophobic polystyrene (PS) derivative. A bottom PMFA/top PS derivative dielectric layer then formed during the spin-casting step. This structure favored charge carrier transport in the bottom-gate OFET because the hydrophobic PS-derivative surface enhanced the crystallinity of the overlying semiconducting material, and the PMFA reduced the leakage current without hindering carrier transport. The semiconductor/semiconductor blends were formed by homogeneously mixing the small molecules and polymer semiconductors, and the polymer semiconductor was used as a binding material to induce crystallization of the small molecule semiconductor. The μ_{FET} values of the OFETs were enhanced up to 5 cm^2/Vs, similar to the values obtained from single-crystal small molecule semiconductor-based OFETs [6].

Although a variety of blending strategies have been tested in an effort to improve the device performances, electrically stable OFETs have not yet been prepared. The electrical stability of an OFET is one of the most important factors for commercialization

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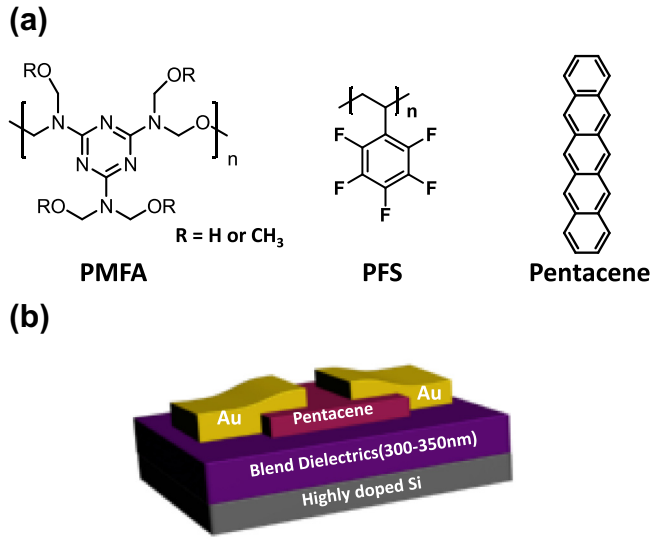

Fig. 1. (a) Chemical structures of PMFA, PFS, and pentacene. (b) Schematic diagram showing the device structures of the OFETs prepared in this study.

because the threshold voltage (V_{th}) shift and the on-current drop that occurs during long operation periods tend to degrade the performances of whole integrated circuits, such as inverters, ring oscillators, and display backplanes [7–10].

Here, we report the preparation of PMFA/polypentafluorostyrene (PFS) blend gate dielectric layers for use in bottom-gate, top-contact OFETs to improve the device stability under continuous gate bias stress conditions (Fig. 1). Although PMFA has robust insulating properties, it is so hydrophilic that it induces charge trapping sites at the semiconductor/dielectric interface, thereby degrading μ_{FET} and increasing the magnitude of the V_{th} shift (ΔV_{th}) under an applied gate bias stress [11]. As a simple solution, the hydrophobic PFS was mixed with PMFA to reduce the hydrophilicity. Fluorinated polymers tend to provide good electrical stability under ambient conditions because of their inherent chemical inertness due to the strong C–F bonds and low polarizability under an applied gate electric field [12–14]. Although OFETs based on blends tend to display a low μ_{FET} due to the decreased crystallinity of the pentacene semiconductor, the 10% blend film-based OFETs showed a negligible ΔV_{th} during the gate bias stress applied over 3 h compared with the PMFA-only dielectric-based OFETs. The low number of charge trapping sites found at the semiconductor/dielectric interface and the stretched exponential function modeling results indicated that the 10% blend films possessed a higher barrier to the creation of charge trapping sites and a narrow distribution of trap depths.

2. Experimental

2.1. Materials and sample preparation

Pentacene, PMFA, and PFS were obtained from Aldrich and Polymer Source Inc. Heavily doped n-type Si wafers were used as gate substrates, cleaned in a piranha solution (70% H_2SO_4:30% H_2O_2) for 20 min at 300 °C, and washed with distilled water immediately prior to applying the polymer coating. The PFS/PMFA blend dielectrics were fabricated on substrates with various blending weight ratios. The concentrations of the PFS/PMFA blend films dissolved in methyl ethyl ketone were properly adjusted to control the thickness to be 334 nm (PFS ratio = 0%), 330 nm (2%), 327 nm (5%), 322 nm (10%), respectively. The solutions were stirred in a N_2-purged glove box (H_2O and O_2 <0.1 ppm) over 3 h to dissolve both polymers completely. After spin-coating, the substrates were heated on a hot plate for 1 h at 120 °C to remove residual solvent and to harden the films. Shadow mask-patterned pentacene active films were deposited onto the gate dielectrics using organic molecular beam deposition (OMBD) techniques (with a deposition rate of 0.1 Å/s; vacuum pressure = 10^{-6} Torr; substrate temperature of 25 °C). An Au layer was thermally evaporated onto the pentacene layer through a shadow mask to yield the top-contact OFET electrodes. The channel length (L) and width (W) were 100 and 1000 μm, respectively.

2.2. Characterization

The topographies of the blended gate dielectric and semiconductor layers were characterized using atomic force microscopy (AFM) (Multimode IIIa, Veeco Inc.). The surface energies of the blended dielectrics were evaluated by measuring the contact angles of the two test liquids, water (θ_{water}) and diiodomethane (θ_{DII}). The dispersion (γ_s^d) and polar components (γ_s^p) of the surface energy were obtained, and the sum of these components yielded the total surface energy (γ_s), based on the equation:

$$1+\cos\ \theta = \frac{2(\gamma_s^d)^{\frac{1}{2}}(\gamma_{lv}^d)^{\frac{1}{2}}}{\gamma_{lv}} + \frac{2(\gamma_s^p)^{\frac{1}{2}}(\gamma_{lv}^p)^{\frac{1}{2}}}{\gamma_{lv}},$$

where γ_{lv} is the surface energy of the test liquid, and γ_{lv}^d and γ_{lv}^p refer to the dispersive and polar components, respectively. The film thickness was determined using ellipsometry (J.A. Woollam. Co. Inc.), and the X-ray diffraction (XRD) data were obtained from 1D-mode XRD spectroscopy measurements collected at the 5A beam line of the Pohang Accelerator Laboratory. The electrical characteristics of the pentacene OFETs were determined in a N_2-purged glove box using Keithley 4200 SCS. The μ_{FET} and V_{th} values in the saturation regime were calculated using the equation $I_d = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_g - V_{th})^2$, where I_d, C_{ox}, and V_g are the drain current, capacitance, and gate voltage, respectively.

3. Results and discussion

Prior to characterizing the OFETs containing PFS/PMFA blend dielectrics, we investigated the dependence of the surface properties on the chemical composition of the blends. Several studies have described the significant role that the dielectric interfacial properties play in determining the electrical performances of OFETs. For example, the surface energy, roughness, and functionalities of the dielectric films substantially influence (a) the seeding structure and orientation of a semiconductor film grown on the substrate, (b) trap formation at the semiconductor/dielectric interface, and (c) the surface potential, which can modulate the carrier density in the channel [15,16]. Specifically, the surface energy and relevant interfacial interactions of the dielectric films were fundamentally important to the overall crystalline structure of the semiconductor films (and the overall device performance), as the competition between the molecule–molecule and molecule–substrate interactions dictated the growth of the thin films [17].

The surface energy depended upon the chemical composition and the packing density of the outmost surface functional groups. The interfacial interactions, including the surface energy, consisted of polar and dispersion contributions, which arose from the presence of permanent dipoles (including hydrogen bonds) and instantaneous dipole moments, respectively. Therefore, the incorporation of non-polar or weakly interacting functional groups led to relatively low surface energies. The inherent characteristics of fluorine (i.e., the small atomic radius comparable to the radius of hydrogen and the low polarizability) notably reduced the surface