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Solution-based self-aligned hybrid organic/metal-oxide complementary logic with megahertz operation

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ABSTRACT

We have developed a novel solution-based integration scheme featuring organic and metal-oxide semiconductors with a polymeric gate dielectric. The integration relies on a facile subtractive patterning technique for the semiconductors, which, through the selection of an appropriate etch stopper, leads to ideal transistor performance. We utilized this novel integration scheme to fabricate self-aligned transistors and logic circuits with a high-mobility p-type conjugated polymer and an n-type amorphous oxide semiconductor, along with a composite polymeric gate dielectric, all solution-deposited by spin coating. The resulting complementary logic gates are capable of rail-to-rail transitions, low-voltage operation down to a 3.5 V power supply, and ample noise margins. Thanks to the self-aligned-gate approach and the state-of-the-art balanced mobilities of the selected semiconductors, our logic gates achieve megahertz operation, thus demonstrating the strength of our hybrid integration scheme.

1. Introduction

The inherent ambipolarity of organic semiconductors has always sustained the promise of all-organic complementary logic circuit integration [1,2]. Bringing together a p- and an n-type organic semiconductor pair on the same substrate would indeed help realize the benefits of silicon-like logic circuits in terms of low power dissipation, robust operation, and ease of design [3]. The promise is yet to be fulfilled in a practical manner, however, as the steady progress towards high-mobility p-type organic semiconductors with excellent air stability is not yet matched fully by the n-type counterpart [4,5]. As a consequence, over the years most investigators resorted to the less desirable unipolar circuit options utilizing one single p-type semiconductor [6–9]. Top-performance implementations of this kind allowed logic-stage propagation delays in the region of the microsecond [7,8]. All-organic complementary circuits have also been demonstrated by a number of groups, inherently giving much larger noise margins and reduced power dissipation [10–12]. The inferior mobilities and stability of the n-type organic semiconductors, however, inevitably led to lower speed performance and reliability with respect to the unipolar p-type-only case.

The concurrent emergence of amorphous metal-oxide semiconductors, featuring a far superior n-type performance and stability, led investigators towards hybrid complementary circuit integration, comprising a metal-oxide in combination with a p-type organic semiconductor [13–16]. The benefits of the complementary approach, together with the choice of top-performance materials from these two classes of semiconductors, generally afforded higher operational speed and reliability than the all-organic complementary counterpart. All these implementations, however, were based on a bottom-gate geometry with an inorganic gate dielectric not processed from solution, and had at most only one of the semiconductors deposited from solution.

In this study we address the challenge of realizing high-speed and top-performance logic within an approach that allows solution processing of both n-type oxide and p-type organic semiconductors and of a compatible low-temperature gate dielectric. Specifically, we present a process flow in which the complementary pair of top-performance solution-processed semiconductors is integrated on the same chip along with a solution-deposited polymeric gate dielectric.

2. Experimental

We achieved complementary integration through a process flow featuring a top-gate, staggered, and self-aligned architecture. The process flow was devised to allow the solution-based deposition of a p-type organic semiconductor (OS) and an n-type amorphous-metal-oxide semiconductor (AMOxS), both processed by spin coating, patterned subtractively, and capped off with a shared polymeric gate dielectric.

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A general illustration of our process flow is shown in Fig. 1. The starting substrate consists of a glass slide on which thermally-evaporated gold source and drain electrodes are defined by photolithography (all patterned with a channel length of $L = 10$ μm and a channel width of $W = 1000$ μm, unless stated otherwise). The amorphous metal-oxide is deposited and patterned first, given its higher processing temperature and superior resistance to solvents, followed by the deposition and patterning of the organic semiconductor. Subsequently, a shared gate dielectric is blanket coated on the sample, and the further processing steps required to achieve the self-aligned gate electrodes are performed as described in [17] (with the aluminum gate electrodes being thermally evaporated through a shadow mask). Finally, circuit connectivity is realized on top of a circuit dielectric (photolithographically patterned S1813™, Shipley Microposit) by opening via holes through it by a combination of photolithography and oxygen-plasma ashing, and by depositing metal interconnects either by thermal evaporation, or from a commercial silver-based ink (TEC-IJ-050, InkTec Co., Ltd.) with a home-built single-nozzle printer.

Both semiconductors are blanket deposited by spin coating, and thus subtractive patterning is necessary to confine each of them to the active areas of their respective TFTs (thin-film transistors). The etching of the amorphous metal-oxide is achieved with diluted hydrochloric acid (by conventional lithography), whereas oxygen-plasma is used for the organic semiconductor. While etching the semiconductors, a suitable etch stopper (ES) is required to protect the active regions of the would-be TFTs. We tested two different etch stoppers, one consisting of a photopatterned micron-thick S1813™ film, and another made of a 35 nm-thick thermally-evaporated aluminum film (patterned through a shadow mask). To avoid damaging the semiconductors during the etch stopper deposition, a 100 nm-thick CYTOP™ (Asahi Glass Co., Ltd.) layer was employed, subsequently patterned by oxygen plasma. At the very end of the semiconductor patterning process, the protective S1813™/aluminum capping off the CYTOP™ islands was stripped by immersion in a suitable solvent (acetonitrile and Shipley's MF-319, respectively), so that the sample could undergo the further steps required for circuit integration.

We implemented this process flow with a particular combination of semiconductors. The organic one we selected is IDT-BT, a top performance p-type polymer which was reported to give hole mobility up to about 2 $cm^2 V^{-1} s^{-1}$ without requiring any high-temperature treatment [18]. The metal-oxide semiconductor used in combination with IDT-BT is a solution-processed alkoxide-based IZO, produced in thin-film form according to the "sol–gel on chip" detailed elsewhere [19,20]. Banger et al. characterized the properties of this metal-oxide in bottom-gate inorganic transistors, demonstrating a semiconducting behavior strongly dependent on process temperature, with mobility values in the region of $2 - 4\ cm^2 V^{-1} s^{-1}$ at the lowest reported process temperatures ($200 - 225$ °C) [19]. In order to have balanced semiconductor mobilities for optimum circuit speed, we utilized a process

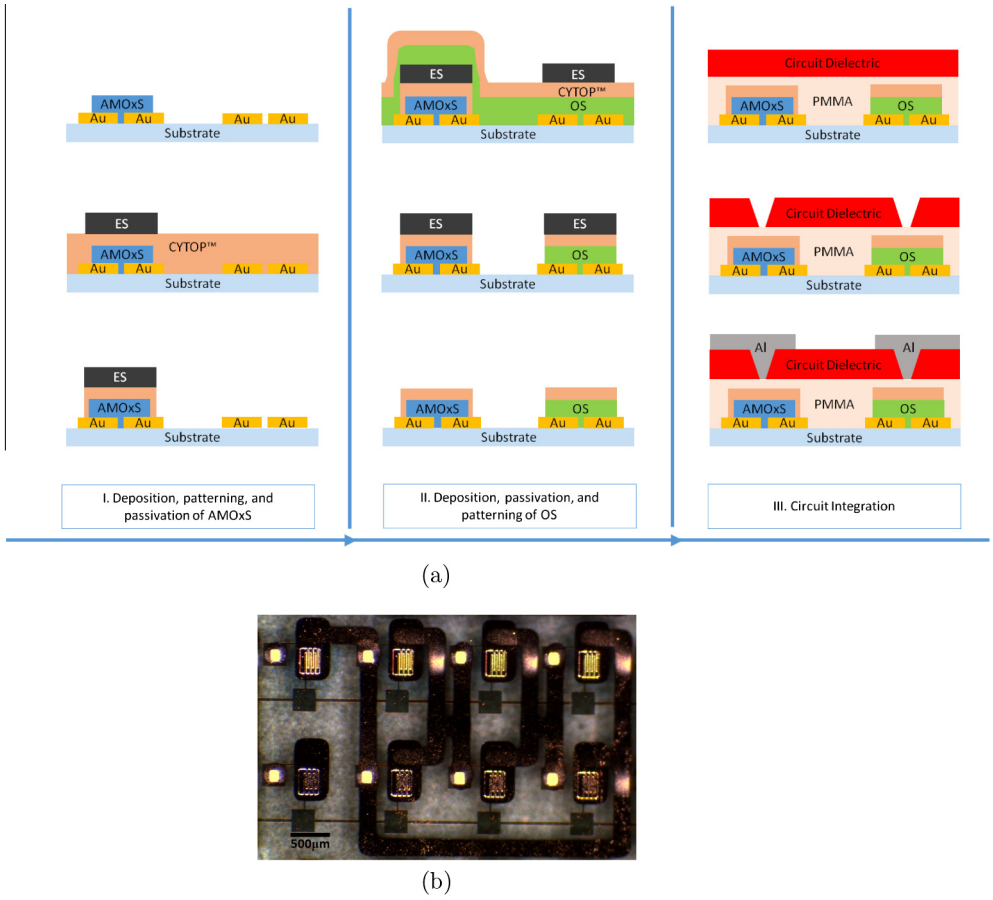

Fig. 1. Schematic process flow (a) and top-view of one of our circuit samples (b). In our process flow, the AMOxS is patterned first (via conventional wet etching), and passivated with CYTOP™/ES before undergoing oxygen plasma. A similar procedure is utilized for the passivation and patterning of the OS. Finally, circuit connectivity is realized by means of metal tracks deposited on the circuit dielectric. The specific circuit shown in (b) is a three-stage ring oscillator, whose performance is detailed in Section 3.