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Mixed-mode cohesive zone parameters for sub-micron scale stacked layers to predict microelectronic device reliability

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ABSTRACT

With continued feature size reduction in microelectronics and with more than a billion transistors on a single integrated circuit (IC), on-chip interconnection has become a challenge in terms of processing-, electrical-, thermal-, and mechanical perspective. Today's high-performance ICs have on-chip back-end-of-line (BEOL) layers that consist of copper traces and vias interspersed with low-*k* dielectric materials. These layers have thicknesses in the range of 100 nm near the transistors and 1000 nm away from the transistors and near the solder bumps. In such BEOL stacks, cracking and/or delamination is a common failure mode due to the low mechanical and adhesive strength of the dielectric materials as well as due to high thermally-induced stresses. However, there are no available cohesive zone models and parameters to study such interfacial cracks in sub-micron thick microelectronic layers.

This work focuses on developing framework based on cohesive zone modeling approach to study interfacial delamination in sub-micron thick layers. Such a framework is then successfully applied to predict microelectronic device reliability. As intentionally creating pre-fabricated cracks in such interfaces is difficult, this work examines a combination of four-point bend and double-cantilever beam tests to create initial cracks and to develop cohesive zone parameters over a range of mode mixity. Similarly, a combination of four-point bend and end-notch flexure tests is used to cover additional range of mode mixity. In these tests, silicon wafers obtained from wafer foundry are used for experimental characterization. The developed parameters are then used in actual microelectronic device to predict the onset and propagation of crack, and the results from such predictions are successfully validated with experimental data.

1. Introduction

Multilayered materials span across a wide-range of applications from aircrafts to microelectronic systems. One of the primary reliability concerns in multilayered material systems is delamination [1,2]. Fracture mechanics based approaches are most often pursued to study delamination [3]. The interfacial fracture mechanics approach assumes a defect of known size along an interface, and the propagation of the initial crack under given loading conditions is studied. Some of the

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Nomenclature

T_n	normal traction (MPa)
T_n^{max}	maximum normal traction (MPa)
δ_n	normal displacement jump in deformation history (μm)
δ_n^*	normal displacement jump at T_n^{max} (μm)
δ_n^c	normal displacement jump at completion of debonding (μm)
D_n	Mode I damage parameter
T_t	tangential traction (MPa)
T_t^{max}	maximum tangential traction (MPa)
δ_t	tangential displacement jump in deformation history (μm)
δ_t^*	tangential displacement jump at T_t^{max} (μm)
δ_t^c	tangential displacement jump at completion of debonding (μm)
G_{Ic}	Mode I strain energy release rate (J/m^2)
G_{IIc}	Mode II strain energy release rate (J/m^2)
G_c	total strain energy release rate (J/m^2)
λ	effective displacement (no units)
β	weighting parameter
D_m	damage parameter
d_m	damage parameter
P	load (N)
L	distance between pins (μm)
E	Young's modulus of silicon substrate (MPa)
H	thickness (μm)
B	width (μm)
v	Poisson's ratio
a	crack length
C	compliance (μm/N)
δ	displacement (μm)
μ	shear modulus (MPa)
Ψ	Mode mixity
γ	fitting parameter

shortcomings of such an approach are multiple simulation models to assess energy available during crack propagation, difficult to model multiple cracks in the same model, inability to predict crack initiation, dependency of the results based on initial crack location and size, etc.

Techniques such as cohesive zone modeling (CZM) or extended finite-element method (XFEM) can alleviate such disadvantages of fracture mechanics approach, mentioned above [4–6]. Advantages of CZM are that it does not require an initial crack, size of the non-linear zone (*K*-dominated zone) need not be negligible in comparison with other dimensions of the cracked geometry [7], and it is a single step simulation process. Over the last few decades, CZM has been successfully implemented to study fracture in metals [8], welded joints [9], concrete [10,11], polymers, functionally graded materials [12,13], adhesively bonded joints in [14,15]. Multimaterial stack numerical analysis using custom material models or in-house programs based on interfacial fracture mechanics and damage evolution laws has also been demonstrated in [16–18]. To be able to implement CZM, the traction–separation parameters should be experimentally characterized. Such experimental characterization is lacking in available literature for sub-micron interfaces over a wide range of mode mixity.

The objectives of this work are to experimentally characterize CZM traction–separation parameters over a range of mode mixity using load–displacement curves of several experiments, to apply such CZM parameters to predict cracking in stacked layers that are approximately 100–1000 nm thick and validate the numerical model using failure analysis results from real devices.

In microelectronics applications, increasingly silicon chips are flipped, placed on organic substrates, and then passed through reflow oven to melt the solder interconnects and thus to bond the silicon chip to the organic substrate. When such a flip-chip assembly is cooled down from lead-free solder melting temperature to room temperature, the mismatch in coefficient of thermal expansion (CTE) between the silicon chip and organic substrate contributes to thermo-mechanical strains and stresses developed in the solder bumps. When the stresses exceed the interfacial adhesion or bulk fracture strength of the interlayer dielectric (ILD) materials located above the solder bumps, delamination in ILD layers occurs. A schematic of forces experienced by a solder bump during reflow and delamination in back end of line (BEOL) stack are illustrated in Fig. 1.