



Space-Filling Supercapacitor Carpets: Highly scalable fractal architecture for energy storage

Athanasios Tiliakos^{a,*}, Alexandra M.I. Trefilov^a, Eugenia Tanasă^b, Adriana Balan^a,
Ioan Stamatin^{a,**}

^a University of Bucharest, Faculty of Physics, 3Nano-SAE Research Centre, 405 Atomistilor Str., Bucharest-Magurele MG-38, 077125, Romania

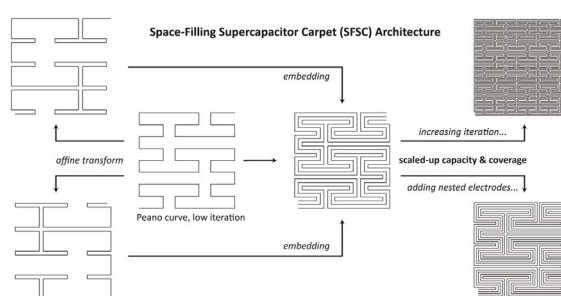
^b Polytechnic University of Bucharest, Faculty of Applied Sciences, Department of Physics, 313 Splaiul Independenței Str., Bucharest, 060042, Romania



HIGHLIGHTS

- Highly scalable architecture for flexible in-plane energy storage devices.
- Fractal electrodes based on the Peano curve of optimal length-to-area distribution.
- Multiple nested electrodes configuration for distributed capacitance effect.
- Improved laser-induced graphene (LIG) method for vector-mode fine-detail printing.
- Competitive advantages due to the geometrical properties of the fractal Peano curve.

GRAPHICAL ABSTRACT



ARTICLE INFO

Keywords:

ECDL supercapacitors
Electrodes
Fractal
Laser-induced graphene (LIG)
Scalability

ABSTRACT

Revamping ground-breaking ideas from fractal geometry, we propose an alternative micro-supercapacitor configuration realized by laser-induced graphene (LIG) foams produced via laser pyrolysis of inexpensive commercial polymers. The Space-Filling Supercapacitor Carpet (SFSC) architecture introduces the concept of nested electrodes based on the pre-fractal Peano space-filling curve, arranged in a symmetrical equilateral setup that incorporates multiple parallel capacitor cells sharing common electrodes for maximum efficiency and optimal length-to-area distribution. We elucidate on the theoretical foundations of the SFSC architecture, and we introduce innovations (high-resolution vector-mode printing) in the LIG method that allow for the realization of flexible and scalable devices based on low iterations of the Peano algorithm. SFSCs exhibit distributed capacitance properties, leading to capacitance, energy, and power ratings proportional to the number of nested electrodes (up to 4.3 mF, 0.4 μWh, and 0.2 mW for the largest tested model of low iteration using aqueous electrolytes), with competitively high energy and power densities. This can pave the road for full scalability in energy storage, reaching beyond the scale of micro-supercapacitors for incorporating into larger and more demanding applications.

1. Introduction

Energy efficiency and sustainability have emerged as strategic

vectors in the initiative against the ongoing energy and climate crises, signatures of the Anthropocene era that initiated with the Industrial Revolution and ushered a profound shift in the relationship between

* Corresponding author.

** Corresponding author.

E-mail addresses: tiliakos@3nanosae.org (A. Tiliakos), istarom@3nanosae.org (I. Stamatin).

humanity and nature [1]. Fossil fuel dependence for energy generation, the high environmental impacts of fossil fuel consumption, and the rapid depletion of exploitable sources have orchestrated an interlocked feedback loop that threatens to derail all associated systems, both economic and ecological [2]. As viable solutions, sustainable energy development strategies involve: intelligent energy consumption on the demand side, energy efficiency on the production side, and replacement of fossil fuels by renewable and alternative energy sources – with the major challenges being the integration of such intermittent sources into the power grid, and their penetration into the transportation sector with its demand for portable energy generation and storage [3]. Parallel to the above, research on energy storage, the intermediate step towards clean and efficient energy usage, has been stimulated by the popularization of portable electronics and electric vehicles, driving the development of storage devices, such as batteries and supercapacitors, towards higher energy and power densities [4].

Supercapacitors (SCs) are rechargeable devices storing energy within the electrochemical double layer (ECDL) at the electrode-electrolyte interface. With larger capacities than conventional capacitors, their charging-discharging rates climb higher than both primary and secondary batteries. SCs are regarded as promising applications in electronics, communications, and transportation, displaying none of the hazards associated with batteries and offering environmental and operational safety alongside a near-infinite cycle life [4,5]. Proposed SC applications include: uninterruptible power supplies (back-up protection against power disruption), load-levelers (back-up power for microelectronics), and auxiliary power sources for electric vehicles in combination with fuel cells or batteries – provided their energy densities can be amplified without sacrificing their high power densities [4–9].

The key requirement for the next generation of SCs has been identified as the capability to maintain conformality (i.e. angle preservation) with deformation while retaining electrochemical functionality: SCs need to be flexible, bendable, foldable, and stretchable to accommodate portable electronic devices, such as wearable electronics, electronic paper, and implantable medical devices [10]. To this end, the classic architecture of conventional SCs has proven prohibitively cumbersome. On the other hand, micro-supercapacitor (MSC) architecture offers considerable potential, concentrating on the following designs: thin film electrodes in a sandwich formation, fiber-shaped electrodes with core-shell structures, and in-plane arrays of micro-electrode digits in a comb-style arrangement [11]. Notably, the in-plane array design registers as a top contender for flexible electronics, as it features the following advantages: the micro-electrode array maximizes the exposure of the active electrode materials to the electrolyte, thus magnifying the power density of the device; the small interspace between microelectrodes and the absence of a separator minimize the electrolyte's ionic resistance; and their small size makes them ideal for microelectromechanical systems (MEMS) and on-chip electronics [11].

Starting from the basis of in-plane design, we interrogate the key parameters of SC form factor: electrode geometry and the efficiency of arrangement within a given surface area [12]. We investigate the linear configuration of electrodes in the comb-array setup, and we consider space-filling curves as an alternative electrode design. Introduced in the 19th century as mathematical oddities, space-filling curves are constructed iteratively as sequences of piecewise linear continuous curves (i.e. real-valued functions defined on the set of real numbers, whose graphs are composed of linear sections), with successive iterations more closely approximating the space-filling limit (i.e. their range contains the entire 2D unit square) [13]. Contrary to popular belief, space-filling curves are not pure fractals: they precede the inception of fractal geometry by roughly a century and, as such, they have been designated as pre-fractals [14]. However, individual iterations of space-filling algorithms can be described using fractal metrics, and high iterations exhibit a trademark fractal property: maximization of the Lebesgue measure of a Euclidean D-space embedded in a dimension D + 1 (e.g.

length maximization of a 1D line embedded within a 2D surface) [14]. On the negative side, these attractive properties and the general allure of fractals have managed to beget a disheartening number of endeavors that misappropriate the concepts of fractal geometry.

The use of fractals and space-filling curves in microelectronics is not a novel idea [15]. In energy storage, capacitors based on the Koch island fractal were proposed as early as in 1998 [16], followed by: quasi-fractal capacitor layouts for CMOS implementations [17], supercapacitors employing carbon particles with a fractal perimeter as electrode materials [18], theoretical investigations of space-filling designs for capacitor and SC electrodes [19,20], and physico-mathematical models of SC behavior based on fractals [5,21]. In communication electronics, fractals and space-filling curves have flourished in implementations of antennas and resonators [22–25], also finding applications in phase shifters [26], multiband reflectors [27], and photonic crystals [28,29]. Furthermore, recent developments have demonstrated the mechanical advantages of space-filling curves in stretchable electronics [30,31].

In this work, we design a nested electrode configuration for SCs based on the Peano space-filling curve, after interrogating the properties of other prospective candidates (H-Tree fractal; Gosper, Hilbert, and Moore curves) and selecting the optimal pattern according to the criteria presented above [32–36]. Space-Filling Supercapacitor Carpets (SFSCs) are laser-printed according to the LIG method, which employs commercial CO₂ laser CNCs to photopyrolyze polyimide (PI) precursors into porous graphitic structures (graphene-based foams) of high electrical conductivity and double-layer capacitance [37–41]. We demonstrate how this fractal architecture can conform to devices of large surface areas while still retaining the planar configuration, thus bridging the scale gap between MSCs and conventional SCs. Due to the plasticity of the PI precursor, the SFSC devices become effectively flexible, with the option of becoming stretchable by transferring to elastomeric substrates [41].

2. Experimental

2.1. Materials and methods

2.1.1. Precursor materials and laser processing

Polyimide (PI) films are commercially available in a variety of brand names (e.g. Apical[®], Kapton[®], Kaptrex[®], Novax[®], Upilex[®]); the LIG method was originally developed using Kapton PI films [37–39]. We opted for single-sided copper-clad laminates (Pyrulux[®] LF9150R, DuPont[™]) of Kapton film (127 μm) on copper foil (13 μm, rolled-annealed), to provide flexural endurance for self-standing devices and minimal deformation at the high temperatures of laser pyrolysis. All surfaces were thoroughly cleaned with isopropanol and DI water prior to laser processing.

The laser printing method was reconfigured to employ single-line continuous scanning (vector-mode) instead of rastering. Care was taken to account for the thermal properties of the support substrate, as they affect LIG printing quality (Sup. Fig. 1, Sup. Table 1). The performance of Pyralux was compared to unclad films (55 μm, Kapton[®] HN, DuPont[™]); Pyralux films proved to withstand higher levels of laser fluence, ranging from 4.4 to 8.8 J mm⁻². To simplify parameterization, the geometrical parameters (width w , interspace distance g) were combined into a single dimensionless packing ratio $\eta = w/(w + g)$ (metallization ratio when referring to conventional electrostatic capacitors [42]). The determinant for printing quality screening was the root mean squared roughness R_{RMS} of LIG lines, which is minimized over high fluence levels at the cost of increased line widths – this is offset by reduced interspace distances, which result in shorter ionic diffusion paths [43]. We opted for the laser parameter combination resulting in a compromise between sufficiently low roughness (R_{RMS} of 13.95, N4 ISO grade) and line dimensions: mean width w of 254.46 μm (SE of 3.2 μm), and interspace distance g of 219.12 μm (SE of 4.73 μm), at a packing ratio η

Download English Version:

<https://daneshyari.com/en/article/7725536>

Download Persian Version:

<https://daneshyari.com/article/7725536>

[Daneshyari.com](https://daneshyari.com)