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Effect of contact area and depth between cell cathode and interconnect on stack performance for planar solid oxide fuel cells☆

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HIGHLIGHTS

- Convex parabolic relation of power density vs. interface contact area and depth was found.
- The degradation rate of stack repeat unit decreased gradually with the increasing contact area.
- The stack repeat unit inside stack appears no degradation with the increasing contact depth.

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ABSTRACT

Effect of contact area and depth between cell cathode and interconnect on output power density and degradation of stack for planar SOFCs has been investigated systematically. The results indicate that the maximum output power density (MOPD) of repeating units inside stack increases firstly and then decreases slightly with the increasing interface contact area and depth, respectively, showing an approximate convex parabolic relation of power density to interface contact area and depth. The degradation rate of repeating units decreases gradually for 972 h' operation under 0.75 V unit-cell voltage, 0.476 A cm^{-2} current density and 41.8% fuel utilization with different contact area. At the optimum value of the interface contact area, the repeating unit inside stack appears no degradation under operation for 1060 h under 0.8 V unit-cell voltage, 0.444 A cm^{-2} current density, and 78% fuel utilization efficiency.

1. Introduction

Solid oxide fuel cells (SOFCs) are highly efficient energy conversion devices. To obtain applicable electric energy, unit cells must be connected in series to form a cell stack [1]. The SOFC stack structure shows that the performance is mainly influenced by metal interconnects, unit cells, and interfaces between unit cells and metal interconnects. For many years, the cell performance has been considered as the fundamental influencing factor for SOFC stack; thus, improving the cell performance has always remained a research interest [2–4]. However, when a high-performance unit cell is used, the SOFC stack still has significantly poorer performance than the unit cell itself [5]. This result indicates the importance of investigating the performance of the interconnect for SOFC stack. According to research findings, if metal materials are used as interconnects for SOFC stack, the resistance of the interconnect is still small under 700 °C–850 °C, and its influence on the output performance of the whole cell stack is almost negligible [6–8]. The interface contact between metal interconnect and unit cell is currently recognized as the key factor influencing the performance of SOFC stack [9,10].

The interface contact between SOFC stack components mainly comes from two aspects: (1) the interface contact between anode and interconnect, and (2) the interface contact between cathode and interconnect. For SOFC stack, the anode functions as a metal material under an operating condition. Therefore, metal–metal contact is mainly on the anode side of the stack. The contact resistance on anode side is almost negligible after full contact is made [11]. Research has also discovered that the contact resistance in SOFC stack mainly comes from the interface contact between cell cathode (perovskite material) and metal interconnect [12–14].

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Thus, to minimize the resistance produced by the interface contact between cell cathode and interconnect, precious metals such as Pt and Ag are used as the current collecting materials on the cathode side [11,15]. Using precious metals as the cathode current collector can provide the cell with higher output power density. However, their high material costs highly limit their large-scale commercial application in SOFC.

The interface contact area between the cell cathode and interconnect is a key factor influencing the output performance for SOFC stack [16–18]. Therefore, with the same materials selected as the cathode current collecting layer (CCCL), increasing the interface contact area between the cell cathode and metal interconnect can significantly increase the power density of the cell inside SOFC stack. For example, the research findings of Jiang et al. [16] in 2003 showed that when the contact area of the cell cathode grew from 5% to 27.5%, the maximum output power density (MOPD) of the cell correspondingly increased from 0.10 W cm^{-2} to 0.52 W cm^{-2}. However, according to the report, the contact area varied within the range of 5%–27%, and the cell area was relative small (5 cm × 5 cm), which were some of the limitations. Furthermore, no research exists on the relationship between the interface contact area and the degradation rate of the cell in the literature [16]. Our preliminary study [19] also provided that the MOPD of the cell inside SOFC stack is related to the interface contact area and contact depth between cell cathode and interconnect. Based on the aforementioned findings, the degradation rate of the cell inside stack shows a direct relationship with the interface contact [20]. However, quantitative research on the relationship of the contact depth between the cell cathode and the metal interconnect with the output performance, especially the relationship with the degradation rate, is severely limited.

This study is a quantitative research on the relationship between interface contact area and depth, as well as between MOPD and degradation rate, by varying the contact area and depth between the cell cathode and the metal interconnect. A preliminary discussion on the specific mechanism is included, providing useful reference for the research and development of an SOFC stack with high power density and low degradation rate.

2. Experimental methods

The anode-supported NiO–YSZ/YSZ/LSM–YSZ unit cells were used in this experiment. The manufacturing process and parameters of the cell are described in detail in the literature [21,22]. In this experiment, the cell size in our stack was 10 cm × 10 cm with an active cathode area of 63 cm^2. Cells were machined to the required size by laser cutting. To realize the full contact between cell anode and metal interconnect, a NiO layer of about 130 μm was printed on the anode side of the cell by screen printing. After drying, a layer of about 250 μm $(La_{0.75}Sr_{0.25})_{0.95}MnO_3$ (LSM) was printed on the cell cathode side by the same method. A stack was assembled according to the schematic diagram, as shown in Fig. 1, in which the metal interconnect was 430 ferritic stainless steel and the sealing material was Al_2O_3–SiO_2–CaO based glass. The performance of the sealing materials is described in the literature [23].

On the anode side of the metal interconnect, a kind of linear-type gas channel was prepared by etching with a depth of about 0.5 mm. On the cathode side of the metal interconnect, metal mesh was used as gas channel and electron collector. The structure of the metal mesh was designed and prepared by punching according to the reported references [24–26], as shown in Fig. 2. In this work, Ni-based alloy material was applied and manufactured as metal mesh, which was welded on the metal interconnect. To prevent high-temperature oxidation and Cr element volatilization, a layer of Ni–Cr/LSM composite coating was sprayed on the cathode side of the metal interconnect by plasma spraying technique. The relevant process indexes can be found in the literature [20].

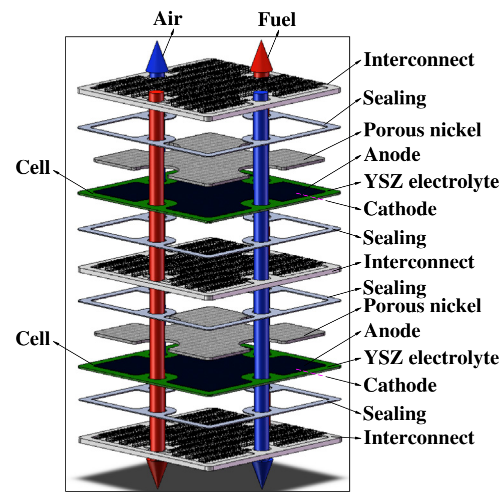

Fig. 1. Schematic diagram of stack assembling.

To study the influence of interface contact area on the output power density and degradation performance of the repeating unit (containing a piece of interconnect and a piece of unit cell) and unit cell inside stack, the interface contact area between the metal interconnect and the cell cathode was designed through adjusting the width and amount of protrusions on metal mesh, as seen in Fig. 2. The interface contact between the metal interconnect and the cell cathode mainly occurred through the protrusion on the metal mesh. Therefore, when the metal mesh made full contact with the cell cathode, the interface contact area was equal to that of the protrusion on the metal mesh. Thus, the interface contact area can be changed by varying the width and number of protrusions on the metal mesh, i.e., varying the values of *a* (width of metal mesh), N_1 and N_2 (amount of protrusions on meal mesh) in Fig. 2). With this interface contact method, the theoretical contact areas were designed as 28.17%, 33.39%, 38.84% and 45.37%, respectively, according to the stack structure shown in Fig. 1. The corresponding parameters were listed in Table 1.

Based on these contact areas, a first 4-cell stack (called stack 1) was assembled to conduct the test. In the stack assembly process, the voltage leads were led out from the anode side and cathode side of the cell, respectively, as shown in Fig. 3. With the voltage leads on both sides of the cell, the independent voltage curve could be obtained for each component inside the stack in the operating

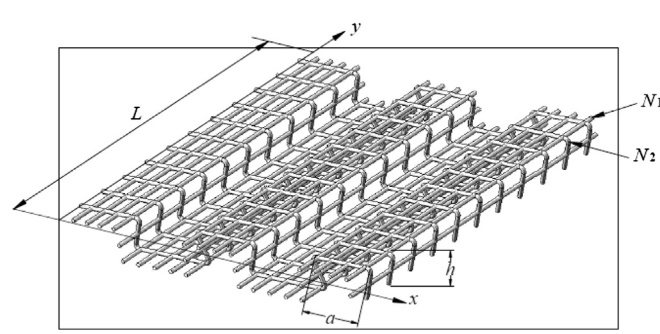

Fig. 2. Schematic diagram of metal mesh on cathode side: *a*–the contact width of metal mesh; *L*–the total length of metal mesh; *h*–the height of metal mesh; N_1–the amount of metal mesh in *y* direction; N_2–the amount of metal mesh in *x* direction.