Journal of Power Sources 232 (2013) 66–73

Contents lists available at SciVerse ScienceDirect

Journal of Power Sources

journal homepage: www.elsevier.com/locate/jpowsour

Sputtered nanocrystalline coating of a low-Cr alloy for solid oxide fuel cell interconnects application

Shujiang Geng [a,b,*], Yaohua Li [a], Zhonghe Ma [a], Shenglong Zhu [b], Fuhui Wang [b]

[a] School of Materials and Metallurgy, Box 119, Northeastern University, 3-11 Wenhua Road, Shenyang 110819, China
[b] State Key Laboratory for Corrosion and Protection, Institute of Metal Research, Chinese Academy of Sciences, 62 Wencui Road, Shenyang 110016, China

HIGHLIGHTS

- Sputtered coating of a low-Cr Fe–Co–Ni alloy with 0.36wt.% Si was prepared.
- Oxidation resistance of the sputtered coating was extremely improved in air at 800 °C.
- The surface scale structure with a low-Cr containing $(Fe,Co)_3O_4$ spinel atop Cr_2O_3 formed on the sputtered coating.
- The spinel layer served as an effective barrier to Cr outward migration.
- The surface scale exhibited a good electrical conductivity.

ARTICLE INFO

Article history:
Received 12 November 2012
Received in revised form
8 January 2013
Accepted 10 January 2013
Available online 21 January 2013

Keywords:
Low-chromium alloy
Sputtered coating
Oxidation
Area specific resistance

ABSTRACT

Sputtered coating of a low-Cr Fe–Co–Ni alloy with 0.36wt.% Si has been prepared on the same cast alloy via magnetron sputtering method. The sputtered low-Cr alloy coating with columnar nanocrystalline structure is thermally oxidized in air at 800 °C corresponding to the cathode atmosphere of solid oxide fuel cell (SOFC). It is found that the oxidation resistance of the sputtered low-Cr alloy coating is significantly improved in comparison with the cast low-Cr alloy. A double-layer oxide scale is thermally developed on the sputtered low-Cr alloy coating after oxidation for 12 weeks. The outer layer is $(Co,Fe)_3O_4$ spinel containing small amount of Ni and Cr. The inner layer is a continuous Cr_2O_3 layer, followed by oxides of $CrNbO_4$ and Nb_2O_5. The surface scale formed on the sputtered coating after 12-week thermal exposure demonstrates an area specific resistance (ASR) of 31.97 mΩ cm^2. The sputtered low-Cr alloy nanocrystaline coating exhibits a promising perspective for intermediate temperature SOFC interconnects application.

1. Introduction

Recently, significant progress has been obtained by reducing thickness of the electrolyte [1,2] or by using novel electrolytes with high oxygen-ion conductivity [3–5] in order to operate a solid oxide fuel cell (SOFC) at intermediate temperatures (600–800 °C). Such progress has made it possible to employ metal alloys as interconnects. Metal alloys are preferable to the traditional $LaCrO_3$-based ceramic interconnect materials [6–8], since they are much cheaper and more formable, allowing for the fabrication of more complex-shaped interconnects.

The metal alloys being explored for interconnect applications included Cr-based [9], Ni-based [10–12] and Fe-based [13–15] alloys. All of them are Cr_2O_3-forming alloys due to the relatively high electrical conductivity of Cr_2O_3, as compared to Al_2O_3 and SiO_2 [7,16]. Nonetheless, the Cr_2O_3-forming alloys have an inherent weakness, i.e. the formation of volatile Cr(VI) species under operating environments of SOFC cathode owing to the Cr_2O_3 evaporation. The volatile Cr(VI) species may migrate to and thus poison the cathode [17], leading to the deterioration of cell performance [18–20]. For metal alloys interconnects, therefore, the formation of a stable, electrically conductive and low-Cr volatility oxide outer layer atop the Cr_2O_3 is highly desirable to resolve the Cr-poisoning issue. Indeed, a novel low-Cr Fe–Co–Ni base alloy has been recently developed for SOFC interconnect applications, which upon thermal exposure forms a double-layer oxide structure with $(Fe,Co,Ni)_3O_4$ spinel as the outer layer and Cr_2O_3 as the inner layer in contact with internal oxides including Si individual oxide

* Corresponding author. School of Materials and Metallurgy, Box 119, Northeastern University, 3-11 Wenhua Road, Shenyang 110819, China. Tel.: +86 24 83673860; fax: +86 24 83687731.
E-mail addresses: gengsj@smm.neu.edu.cn, gengshujiang@yahoo.com (S. Geng).

0378-7753/$ – see front matter © 2013 Elsevier B.V. All rights reserved.
http://dx.doi.org/10.1016/j.jpowsour.2013.01.067

particles [21]. The double-layer oxide structure demonstrated an excellent oxidation resistance and electrical conductivity. Importantly, the spinel outer layer significantly blocked the Cr volatility from the inner layer of Cr_2O_3. However, Si with content of 1.5wt.% at least must be added into the low-Cr alloy in order to promote the formation of a continuous Cr_2O_3 inner layer. Hence, the potential challenge for this alloy is that the discrete internal oxide particles of SiO_2 underneath Cr_2O_3 layer might become a continuous layer which has a quite high electrical resistivity, subsequently resulting in stack malfunction.

In order to avoid the formation of a continuous SiO_2 layer, a similar low-Cr alloy with 0.36 wt.%Si which is an acceptable level for SOFC interconnect applications have been made. A columnar nanocrystalline coating was deposited on the cast low-Cr alloy with identical composition by means of magnetron sputtering method. The short-term oxidation behavior of the sputtered low-Cr alloy coating indicated that a double-layer oxide structure with an outer layer consisted mainly of $(Co,Fe)_3O_4$ spinel atop an inner layer of Cr_2O_3 was thermally grown [22], even though the content of Si was much lower than 1.5wt.%. In this paper, details regarding long-term oxidation behavior and surface scale electrical conductivity of the sputtered low-Cr alloy nanocrystalline coating are evaluated and discussed in air at 800 °C corresponding to the SOFC cathode environment.

2. Experimental

A low-Cr Fe–Co–Ni base alloy with chemical composition (in weight percent) of 30.3% Co, 24.03% Ni, 5.71% Cr, 4.62% Nb, 0.36% Si, 0.053% Y, <0.05% Mn, 0.0023% P, 0.0034% C, <0.001% S, and the balance Fe, was prepared in a vacuum-induction furnace. The samples (15 × 10 × 1.5 mm) used as the substrate for coating deposition were cut from an ingot by an electric-discharge machining (EDM). After drilling a hole with a diameter of 1.5 mm in the upper center of the sample, each sample was ground to 600-grit with silicon carbide papers. Then they were sandblasted, followed by ultrasonic cleaning in acetone before sputtering. The target was the identical cast low-Cr alloy sheet of 248 × 124 mm^2. The sputtering deposition was conducted for 24 h with argon pressure of 0.12 Pa, substrate heating temperature of 180 °C and the sputtering target DC power of 1.2 kW. The substrate samples for coating were rotating in front of the target during sputtering so that all sides of the sample were deposited uniformly.

The thermal expansion behavior of the low-Cr Fe–Co–Ni alloy with 0.36wt.% Si was measured using a dilatometer with rectangle bar (length, 8 mm; width, 1 mm; height, 1 mm). The thermal expansion measurement was conducted from 50 to 800 °C in air.

Oxidation testing of both the cast alloy and its sputtered nanocrystalline coating was conducted in a box furnace. The samples were hung in alumina crucibles. The cast alloys were oxidized in air at 800 °C for total 6 weeks, and the sputtered coatings were oxidized for total 12 weeks. The weight of each sample was measured after furnace cooling to room temperature following each 1-week thermal exposure.

The surface and cross-section morphologies of the samples were observed by scanning electron microscopy (SEM) with an energy dispersive X-ray spectroscopy (EDX). The sputtered coating was examined using transmission electron microscopy (TEM) to determine the size of the columnar grain. The phase structures of the samples were identified with X-ray diffraction (XRD).

Electrical resistance of oxidized samples was measured between 600 and 800 °C in air using 4-point method. The measurement setup was described in our previous work [23]. Two of the oxidized surfaces were covered with Pt paste, followed by curing at 800 °C in air for 1 h. Each Pt foil had two welded Pt leads. Two alumina rods and springs were used to apply pressure and clamp the assembly together during measurement. A constant current of 10 mA (I) was applied across two Pt leads by a current source, and then the corresponding voltage (V) across the other two leads was measured by a multimeter. The resistance (R) was calculated according to the Ohm's law, $R = V/2I$. A factor of 2 was included to account for the measured voltage across two oxide scales. The area specific resistance (ASR) of the oxide scale was then equal to R multiplied by the area covered by the Pt paste.

3. Results and discussion

3.1. Thermal expansion behavior of the low-Cr alloy

Fig. 1 shows the thermal expansion behavior of this low-Cr alloy with 0.36wt.% Si. It exhibited a good match in thermal expansion behavior with other cell components, including the electrolyte, cathode and anode in the temperature range of 200–800 °C, similar to that of the low-Cr alloy with 1.5wt.% Si [21], indicating that the decrease of Si content from 1.5wt.% to 0.36wt.% did not obviously influence the thermal expansion behavior of the low-Cr alloy.

3.2. Characterization of the sputtered coating

The SEM surface morphology of the sputtered low-Cr alloy coating is shown in Fig. 2. The surface appearance of the sputtered coating looks like cauliflowers with columnar grain structure, and the diameter of the columnar grain is lower than 10 nm, as demonstrated in the inserted images including the SEM fractured cross-section and TEM bright field micrograph. It was concluded that the low-Cr alloy sputtered coating was composed of the columnar nano-grains. Moreover, the phase structure of the sputtered coating is the same as its cast alloy [22]. Clearly, a large number of interfaces were observable between different cauliflowers, which were also present between columnar grains from the SEM cross-section view. It was the interfaces or grain boundaries that significantly changed the oxidation behavior of the sputtered coating upon thermal exposure in the environment of SOFC cathode as discussed later.

3.3. Oxidation behavior

3.3.1. Oxidation kinetics

Fig. 3 depicts the mass gain of the sputtered low-Cr alloy nanocrystalline coating as a function of oxidation time in air at

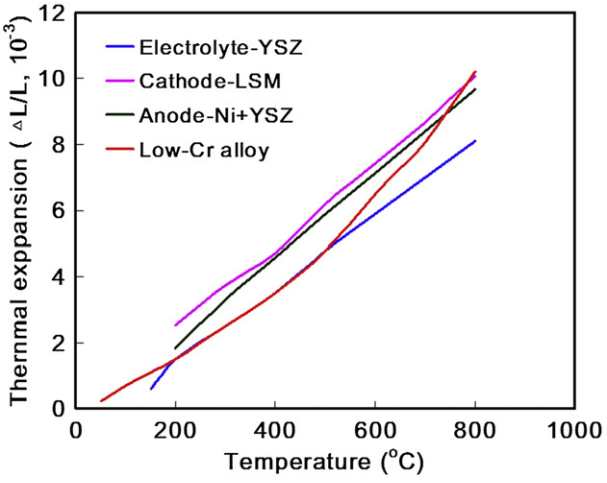

Fig. 1. Thermal expansion vs. temperature for the low-Cr alloy with 0.36wt.% Si, as compared to other cell components.