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Low temperature dielectric properties of $Ce_{0.8}Gd_{0.2}O_{1.9}$ films

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ABSTRACT

Although Gd-doped ceria is one of the most important and well-studied of oxygen ion conductors, the relationship between its mechanical and electrical properties is not completely understood. In particular the low temperature electrical behavior of Gd-doped ceria, and its response to mechanical strain, have not been characterized. We have used impedance spectroscopy (1 Hz–1 MHz) to investigate the dielectric properties of both Si substrate-supported and self-supported $Ce_{0.8}Gd_{0.2}O_{1.9}$ thin (450 ± 50 nm) films in the temperature range of 35–440 K. We find that the grain boundary electronic conductivity for both types of $Ce_{0.8}Gd_{0.2}O_{1.9}$ films freezes out between 120 and 150 K. Upon cooling to 40 K, the effective dielectric constant of the substrate-supported films decreases uniformly, remaining within the range of 20.5 ± 2.5. In contrast, all (17) self-supported films investigated exhibit small (~2%) but readily detectable instability of the dielectric constant between 80 and 140 K. Furthermore, below 90 K, the dielectric constant of the self-supported films depends on the applied voltage and displays hysteretic behavior. This strongly suggests that even below 100 K, the self-supported films can undergo structural changes. Comparison of the lattice parameter at 300 K and at 100 K shows that the self-supported films contract upon cooling with a thermal expansion coefficient close to that of the bulk material, whereas the substrate-supported films exhibit a thermal expansion coefficient which is approximately twice as large. On the basis of our earlier findings concerning the inelastic behavior of Gd-doped ceria films, we propose that a probable explanation for the observed differences between the self-supported and the substrate-supported films is that in the self-supported films, oxygen vacancy-cerium complexes are able to undergo partial ordering. In substrate-supported films these changes are suppressed by the tensile strain imposed by the substrate upon cooling.

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1. Introduction

Cerium oxide, in both pure and doped forms, exhibits a number of unusual and important properties including ionic conductivity due to the high mobility of oxygen vacancies; a series of different phases formed upon reduction [1]; dependence of the lattice parameter and electrical properties on grain size [2]; and non-linear elastic effects, which have been named "chemical stress" [3] and "chemical strain" [4–7]. The term "chemical strain" has been given to materials which display time-scale dependent elastic moduli attributed to the internal reorganization of point defects [4–9]. Although most investigations have been performed at high temperature [10–12], during the last few years the properties of doped ceria at or somewhat above room temperature have also become a subject of interest. These studies were primarily motivated by two questions. First, the oxygen ion conductivity below 200 °C remains largely uncharacterized because it is obscured by electronic and proton conductivity [13–17]. Second, below 200 °C, 20 mol% Gd-doped ceria $Ce_{0.8}Gd_{0.2}O_{1.9}$ was found to exhibit strong deviation from linear elasticity, which extended X-ray absorption fine structure spectroscopy (EXAFS) was able to relate to local distortions of the fluorite lattice [6,7]. These distortions were attributed to the interaction of oxygen vacancies and Ce^{4+} ions, which is significant between 200 °C and room temperature and which is sensitive to external constraints, i.e. strain. In this view, comparing the dielectric properties of strain-free, self-supported films [4,5,18,19] with those of substrate-supported films, which acquire strain upon cooling, [20–22] may add to our understanding of the relationship between the mechanical and electrical properties of Gd-doped ceria. In particular, the low temperature electrical behavior of $Ce_{0.8}Gd_{0.2}O_{1.9}$, and its response to mechanical strain may shed light on the characteristic energy of the local lattice distortions. Furthermore, at cryogenic temperatures, the contribution of the grain boundaries to the dielectric response should be sufficiently small to permit observation of effects related to interaction of point defects, if they are present.

2. Experimental

Substrate-supported 450 ± 20 nm thick films of $Ce_{0.8}Gd_{0.2}O_{1.9}$ were prepared by sputtering from stoichiometric targets onto a

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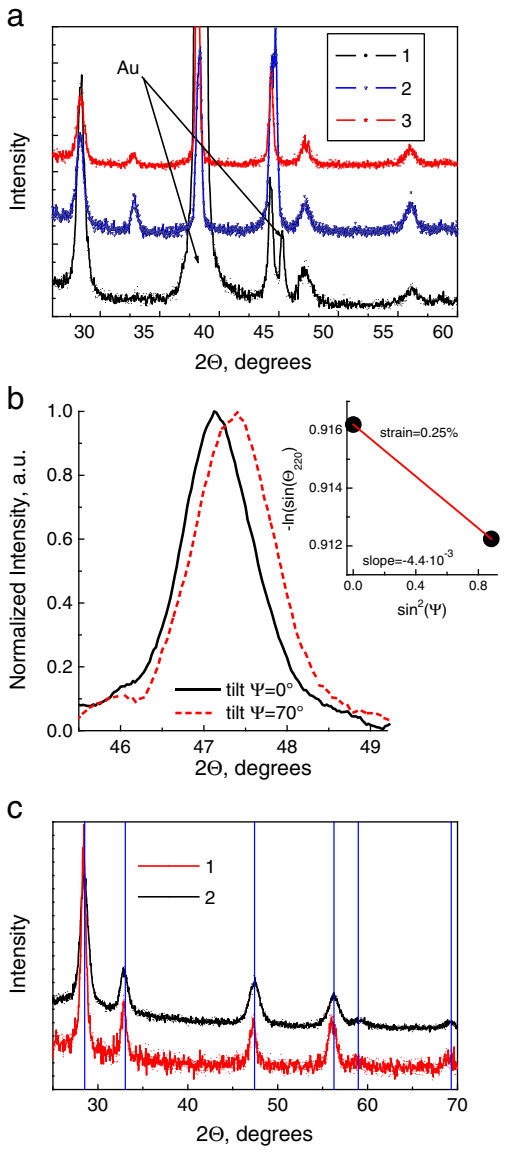

Fig. 1. a) Room temperature XRD patterns of a $Ce_{0.8}Gd_{0.2}O_{1.9}$ film on Si\Au with $\Psi = 0°$ (line1), 45° (line 2) and 70° (line 3) tilts. Diffraction peaks due to the Au contacts are marked with arrows; b) Room temperature XRD patterns of the 220 diffraction peak of a $Ce_{0.8}Gd_{0.2}O_{1.9}$ film on Si\SiO_2 with $\Psi = 0°$ (line1) and 70° (line 2) tilts; Inset: dependence of $-\ln(\sin\Theta_{220})$ vs $\sin^2(\Psi)$ indicating that the film is strained [29]. The Poisson ratio used to calculate that strain $\nu = 0.22$ [3,30]; c) Transmission XRD pattern of a self-supported $Ce_{0.8}Gd_{0.2}O_{1.9}$ film (line 1). The film was prepared by partial substrate removal of the film whose diffraction is shown in b). The XRD pattern of a substrate-supported film with a $\Psi = 70°$ tilt is shown for comparison (line 2). These diffraction patterns were measured prior to the deposition of the Au contacts. Vertical lines denote the standard powder diffraction pattern of $Ce_{0.8}Gd_{0.2}O_{1.9}$ [31].

(100)-Si substrate covered by a 200 nm thick layer of Au prepared by electron beam evaporation. Au was chosen because of its chemical inertness and ductility; it allows complete stress and strain relaxation, which is difficult to achieve with other substrates. The sputtering gas was a 1:1 mixture of Ar and O_2. To eliminate oxygen deficiency, the films were annealed in air at 550 °C for 4 h. The X-ray powder diffraction (XRD) patterns, acquired with a TTRAX-III theta-theta diffractometer (Rigaku, Japan) at film inclination angles of of 0, 45 and 70°, showed that the positions of diffraction peaks do not depend on the inclination angle (Fig. 1a). Peak positions were determined with Voigt profile fitting using Jade 9 software (MDI, CA). This indicates that the annealed substrate-supported films were strain free at room temperature. The room temperature unit cell constant of the substrate-supported films was $a_s = 5.458 \pm 0.002$ Å; peak intensities and line widths indicate that the films have a weak (111) texture and grain size of 15–40 nm. SEM micrographs show that the films were pore free. After annealing, 200 nm thick, 2×2 mm^2 top Au contacts were prepared by electron beam evaporation through a shadow mask.

The self-supported films were prepared by a multistage process shown in Fig. 2. It includes sputtering of a 450 ± 50 nm thick film of $Ce_{0.8}Gd_{0.2}O_{1.9}$ onto a Si wafer covered by a 6.0–7.0 μm thick, thermally grown SiO_2 layer (Fig. 3). 200–240 μm square windows were formed on both the top and bottom surfaces by wet etching (stage 2–3 in Fig. 2). After the deposition of $Ce_{0.8}Gd_{0.2}O_{1.9}$ and annealing in air at 550 °C for 4 h, the films were stress-free (<50 MPa) but not strain-free because of the inelastic behavior due to the chemical strain effect [4,5]. According to XRD measurements, the compressive strain remaining in the films following annealing was 0.2–0.4% (Fig. 1b) [4,5]. The self-supported films were formed by partial substrate removal with deep reactive plasma etching (DRIE) (SF_6, C_4F_8 and O_2) (stage 4–5 in Fig. 2). The last stage of the etching process was carried out without electrical bias on the wafer in order to minimize the sputtering effect. Then the top and bottom Au 200 nm thick lithographically-defined contacts were prepared by electron beam evaporation (stage 5–6 in Fig. 2c). The top image of a complete sample is shown in Fig. 4. To exclude the influence of contact metals, two self-supported films were prepared with Ag contacts. No difference between Au and Ag contacts was observed and all data presented below were obtained with Au contacts. The self-supported films buckled upon substrate removal. The wafers were cut into 4×4 mm squares, each containing one self-supported film, which were then glued with silver paint onto standard ceramic chip carriers. The Au (or Ag) contacts were wire-bonded to the carrier pads with Au wire. The bonding pads were located less than 0.5 mm from the self-supported part of the film and the Au wire lengths did not exceed 3 mm. The part of the contact that extended from the self-supported film onto the SiO_2 layer (Figs. 2–6 and 4) forms a parasitic capacitance. For the films under consideration, this capacitance was found by measuring the capacitance of the structure in which the self-supported part of the $Ce_{0.8}Gd_{0.2}O_{1.9}$ film had been removed. In all

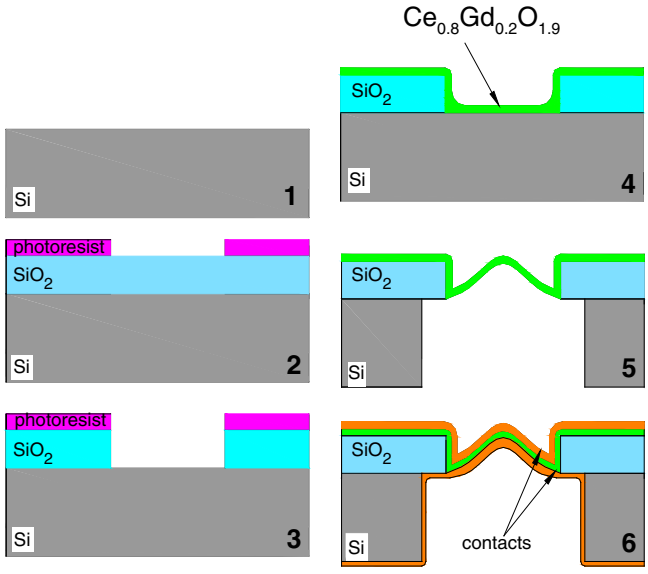

Fig. 2. Preparation of self-supported $Ce_{0.8}Gd_{0.2}O_{1.9}$ film : 1 – silicon (Si) wafer, thickness 300 μm; 2 – thermal oxidation: SiO_2 layer thickness ~7 μm and lithography mask for etching; 3 – wet etch of SiO_2; 4 – sputtering of $Ce_{0.8}Gd_{0.2}O_{1.9}$ film, thickness (450 ± 50 nm); 5 – partial substrate removal by DRIE; 6 – contact deposition by e-beam evaporation. The thickness and resulting resistance of the SiO_2 layer eliminates the substrate-supported region of the sample from the impedance measurements.

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