Nanoscale doping profiles within CdTe grain boundaries and at the CdS/CdTe interface revealed by atom probe tomography and STEM EBIC ☆

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ABSTRACT

Segregated elements and their diffusion profiles within grain boundaries and interfaces resulting from post deposition heat treatments are revealed using atom probe tomography (APT), scanning transmission electron microscopy (STEM), and electron beam induced current (EBIC) techniques. The results demonstrate how these techniques complement each other to provide conclusive evidence for locations of space charge regions and mechanisms that create them at the nanoscale. Most importantly, a Cl dopant profile that extends ∼5 nm into CdTe grains interfacing the CdS is shown using APT and STEM synergy, which has been shown to push the pn-junction into the CdTe layer indicative of a homojunction (revealed by STEM EBIC). In addition, Cu and Cl concentrations within grain boundaries within several nms and μms from the CdS/CdTe interface are compared, Na segregation of < 0.1% is detected, and S variations of ∼1–3% are witnessed between CdTe grains close to the CdS/CdTe interface. The segregation and diffusion of these elements have a direct impact on the material properties, such as band gap energy and n/p type properties. Optimization of the interfacial and grain boundary doping will lead to higher efficiency solar cells.

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1. Introduction

CdTe based solar cells are currently one of the leading commercialized thin-film solar technologies in terms of price per watt and total watts installed per year. The advantage of thin-film CdTe technology over traditional Si is the ability to reduce costs associated with semiconducting material, thus reducing the total module price. However, unlike Si, there is a large efficiency gap between the record CdTe efficiency (21.5%) and the theoretical efficiency (∼33%) [1]. If this gap can be bridged without increasing the production costs, the price per watt of the manufactured modules will reduce significantly. Despite improvements in recent years, the main issue limiting the efficiency of CdTe solar cells is the low value for the open circuit voltage (Voc) (877 mV for the record cell), which is 61% of the band gap, while a similar band gap material, GaAs, has a record cell Voc that is 79% of its band gap [1]. The introduction of Cu into the material is one factor in increasing the Voc due to p-type doping and a better ohmic back contact, but the Cu incorporation begins to self-compensate the p-type doping above a certain incorporation concentration, thus making heavy p-type doping difficult [2–6]. Overall, the low Voc has been attributed to low p-type doping concentrations in the CdTe absorber, a poor back contact, a poor junction with CdS, and electron-hole recombination at point defects, interfaces, and grain boundaries (GBs) [7]. Despite the low Voc, CdTe solar cells have been able to achieve a short-circuit current (Jsc) close to the theoretical

maximum, which is significantly enhanced by the $CdCl_2$ heat treatment (HT) [7,8]. Although Cl segregation at grain boundaries (GBs) and the CdTe/CdS interface after this treatment has been identified using scanning transmission electron microscopy (STEM) electron energy loss spectroscopy (EELS) and STEM energy dispersive x-ray spectroscopy (EDS) techniques, quantification of this segregation is difficult, and low levels of segregation that can be responsible for doping are undetectable with these experiments [9–12]. APT has been used in several papers to characterize CdTe solar cells with higher detection limits, particularly GBs in the CdTe layer, but there has not been a detailed evaluation of the CdS/CdTe interface for this material system to date [6,13–18]. To this end, several regions of fully treated ($CdCl_2$ and Cu) and untreated CdTe devices have been analyzed using atom probe tomography (APT) and compared to SEM electron beam induced current (EBIC) and STEM techniques (including STEM EBIC) to better quantify, understand, and correlate the segregation of Cu and Cl to the device properties, such as the position of space–charge–regions. These results exemplify the advantages of APT over traditional high-resolution characterization methods, and show how APT can be complimentary to other techniques, such as STEM and EBIC, to answer important material questions and verify other significant results.

2. Experimental section

2.1. APT

APT is a technique that has been widely used for the characterization of metallic materials for more than 3 decades [19,20]. Recently, the local electrode atom probe (LEAP) with laser pulsing capabilities was invented and commercialized, which has enabled APT to characterize semiconducting and insulating materials at a larger scale. APT is a time of flight (TOFF) mass spectrometry technique, in which the material of interest is formed into a needle shape and is ideally evaporated one ion at a time, while each ion is projected onto a 2 dimensional position sensitive detector. The information from the detector can be reconstructed by a computer, which results in a data set that includes the 3D atomic positions with up to sub-nm resolution, the identity of each atom, and a low background noise, in which down to 10 ppm of an element can be detected [19]. For CdTe, the background noise can be higher than normal for typical APT experiments because most of the elements evaporate as complex molecules with several mass-to-charge (m/q) peaks. In addition, slight thermal tails, due to the insulating properties of these materials at low temperature, also increase the background [14,16]. Despite these, the background noise is much lower than all other 1 nm or lower resolution techniques. The combination of high resolution and low background noise give this technique its unique properties and edge over traditional high-resolution techniques for the characterization of solar cell materials, specifically the location of dopant profiles in GBs and interfaces.

An FEI Nova 200 dual beam focused ion beam (FIB) was used to lift out and prepare atom probe needles. The wedge lift out geometry was used to mount multiple samples on a Si microtip coupon, which enables for the fabrication of multiple needles from one lift-out [21]. A 5 kV final polishing step was used to minimize Ga damage and sharpen the needle within the region of interest. The very narrow needle dimensions ($\sim$50 nm tip radius, 5° shank angle, 100–500 nm long) and respectively large grain size of CdTe (1–4 μm) make it challenging to encompass a GB in the center of the needle. To this end, several needles were fabricated and evaporated in the atom probe to obtain a few high quality data sets with the desired ROI. The sample preparation method used for the CdS/CdTe interface requires a few additional steps beyond the standard

sample preparation methods, and therefore, a more detailed sample preparation description can be found in Ref. [22].

APT was performed with a local electrode atom probe (CAMECA instruments LEAP 4000X HR) equipped with an energy compensated reflectron lens. The APT needles were run at a base temperature of 30 K, applying 355 nm wavelength $\sim$10 ps laser pulses of 3 pJ, a repetition rate of 100 kHz, and a detection rate of 0.5–1.0%. Data reconstruction and analysis was performed with IVAS 3.6.8. Peak overlaps between $^{130}Te^{2+}$, $^{126}Te^{2+}$ and $^{63}Cu^+$, $^{65}Cu^+$ do exist, but the Cu content could be realized via the peak deconvolution method, which is explained in more detail in Ref. [22].

2.2. Sample growth

All CdTe layers for the samples used in this study were grown by the closed spaced sublimation (CSS) method in the superstrate configuration, which is a high temperature growth method ($\sim$600 C substrate temperature). The CdS/CdTe cells were grown on SnO_2:F/SnO_2-coated low-iron–soda–lime glass substrates (TEC15M), supplied by NSG North America. Roughly 80 nm thick CdS window layers were grown by radio frequency magnetron sputtering using a 4N purity (99.99%) target supplied from Materion. The Cu impurity level of this material was measured to be 0.69 ppm by using spectrographic analysis. After CdS, 4–5 μm CdTe absorber layers (4–5 μm) were prepared by CSS using a 99.999% purity CdTe source materials also supplied by Materion. The Cu impurity level of this source was measured to be < 1 ppm using spectrographic analysis by Materion. Further details of the optimized growth conditions, such as substrate temperature, have been reported elsewhere [23].

2.3. STEM

A 5th order aberration corrected Nion UltraSTEM 200 equipped with a Gatan Enfinium EELS Spectrometer was used for the STEM ADF and EELS measurements, which was operated at an accelerating voltage of 200 kV and a beam current of $\sim$30 pA. For STEM EBIC measurements, the probe current was increased by an order of magnitude to increase the signal to noise ratio. The specimens were thinned using argon ion milling at liquid nitrogen temperature to avoid damage and diffusion due to excessive heating. An $\sim$63 mrad inner angle was used for the HAADF detector with an $\sim$36 mrad EELS collection angle. Cl L23, Cd M45, and Te M45 edges were used for the EELS elemental maps.

2.4. EBIC

The SEM-EBIC measurements were done using a Hitachi S4800-CFEG equipped with a Gatan SmartEBIC system. All EBIC specimens were cross-section argon ion milled at liquid nitrogen temperatures using a Gatan Illion+ system to ensure a smooth, relatively damage free surface. The argon beam acceleration voltage of 5 kV allowed for < 10 nm of the surface to be damaged, as calculated using SRIM simulations [24,25]. After cross-section argon ion milling, the devices were mounted on the Gatan EBIC stage, and connected to a Stanford Research Intruments SR570 low-noise current amplifier. A 3 kV accelerating voltage and beam current of $\sim$30–50 pA was used to ensure a high-resolution probe, while maintaining low-injection conditions [26]. These low accelerating voltage conditions make the EBIC signal sensitive to the magnitude of local electric fields so that space charge regions at the CdS/CdTe interface and GBs can be easily imaged [27]. All EBIC measurements represent the short circuit carrier extraction efficiencies because they were all done without a bias. Further details of the SEM EBIC experiments can be found in the experimental and supplementary materials sections of Ref. [8].