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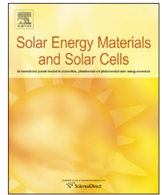

Changes in the current density–voltage and external quantum efficiency characteristics of n-type single-crystalline silicon photovoltaic modules with a rear-side emitter undergoing potential-induced degradation

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ABSTRACT

This study addresses the potential-induced degradation (PID) of n-type single-crystalline silicon (sc-Si) photovoltaic (PV) modules with a rear-side emitter. The n-type rear-emitter module configurations were fabricated using n-type bifacial sc-Si solar cells by module lamination with the p^+ emitter side down. After the PID tests applying -1000 V, the modules show a rapid decrease in the open-circuit voltage (V_{oc}), followed by relatively slower reductions in the fill factor and the short-circuit current density (J_{sc}). Their dark current density–voltage (J–V) data and external quantum efficiencies (EQEs) indicate that the drop in V_{oc} is caused by an increase in the saturation current density due to the enhanced surface recombination of minority carriers. In contrast, the modules exhibit slight degradation under $+1000$ V, which is characterized by only slight decreases in V_{oc} and J_{sc}. The EQE measurement reveals that these decreases are also attributed to the enhanced surface recombination of minority carriers. This behavior is almost identical to that of the polarization effect in n-type interdigitated back contact PV modules reported in a previous study. By comparing the PID resistance with that of other types of modules, the n-type rear-emitter PV modules are relatively resistant to PID. This may become an advantage of the n-type rear-emitter PV modules.

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1. Introduction

The n-type crystalline silicon (c-Si)-wafer-based solar cells attracted attention owing to their high efficiency potential [1]. As for the p^+ emitter formation in the n-type c-Si solar cells, some different techniques were successfully developed, such as boron-diffused front emitters [2,3], p-type/i-type amorphous silicon heterojunctions [4–6], and aluminum (Al)-alloyed rear emitters [7–9]. In particular, the Al-alloyed rear emitters can reduce the production costs since the emitters can be formed by the conventional fabrication process for back-surface fields, which was already widely used in the production of the commercial p-type c-Si solar cells. Therefore, Al-alloyed rear-side emitter solar cells are suitable for use in photovoltaic (PV) power plants, such as very large-scale PV (VLS-PV) systems.

To ensure high reliability and long-term stability of PV systems, it is important to understand the possible degradation behavior of the PV modules. In particular, degradation associated with system bias voltage is identified as a central problem in VLS-PV systems with remarkably high system voltage. This degradation is induced by high electrical potential differences between grounded frames and cells, and it is generally referred to as potential-induced degradation (PID). Thereby, modules deployed in the systems can show significant performance losses [10–12].

The PID of p-type c-Si PV modules was well documented by many researchers. In p-type c-Si modules, significant degradation occurs only under negative potential differences from the grounded frames [10–12]. Such negative potential differences result in sodium cations (Na^+) transfer from the cover glass toward the cells, and the Na^+ accumulates on the devices [12]. (There are controversial points on true Na sources. For instance, an experimental result suggests that Na originates from contaminants on the cell surface [13].) In this situation, the Na^+ ions can easily pass even through SiN_x passivation layers, which are known as good diffusion barriers for sodium [14], with the assistance of a strong electric field [15]. The cells contaminated with Na exhibit a reduction in parallel resistance (R_p) [10] and enhancement of depletion-region recombination [16,17]. This kind of PID is generally referred to as the “PID of shunting type” (“PID-s”) [18]. With regard to these facts,

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Naumann et al. [19] discovered that Na accumulates into the silicon nitride (SiN_x)/Si interface of c-Si solar cells in PID-affected regions. It was also reported that both PID shunts and Na accumulation locally occur at the same spots [20,21]. Moreover, stacking faults existing near the front surface of c-Si were seen to be decorated by Na, and the Na-decorated stacking faults were found to play a crucial role in PID [22]. Naumann et al. and coworkers proposed a physical model that can explain the shunting based on Na-decorated intrinsic stacking faults [18,22,23]. Recently, Ziebarth et al. [24] discussed in detail the diffusion of Na in the intrinsic staking faults and the short-circuiting of p–n junctions by theoretical calculations based on density functional theory and reported their theoretical findings to be consistent with the experimental results presented by Naumann et al. [18,22].

Regarding the PID of the n-type PV modules, there are several studies on interdigitated back contact (IBC) [25–27] and front-emitter [28] PV modules. It was reported that n-type IBC PV modules degrade under positive bias and that PID-affected modules show decreased open-circuit voltage (V_{oc}) and short-circuit current density (J_{sc}) due to the enhanced surface recombination of minority carriers [25]. Naumann et al. showed that n-type IBC PV modules can also degrade under negative bias [26]. In n-type IBC PV modules with a front-floating emitter, a similar degradation was observed under negative bias [27]. Hara et al. [28] revealed that the degradation of front-emitter PV modules occurs under negative bias. They found that the n-type front-emitter modules exhibit decreases in V_{oc} and J_{sc}, while maintaining fill factor (FF), and the degradation tends to occur easily under low temperature or a low bias voltage compared with conventional p-type c-Si modules. By contrast, the PID of the n-type rear-emitter configurations has not been investigated in detail so far.

Herein, using a PID acceleration test, we study in detail the PID behavior of modules with a rear-side emitter. To this end, we fabricated rear-emitter configurations by placing n-type single-crystalline Si (sc-Si) bifacial solar cells with the rear side up. This investigated structure is exactly the same as the Al-alloyed rear-side emitter cells except for the formation technique of the p^+ emitters and the rear-side electrode material and shape. Pingel et al. [29] already reported on the PID of the n-type c-Si bifacial PV modules; however, they focused mainly on the recovery phenomena of the modules degraded by negative bias. In this contribution, we deal with in detail changes in the current density–voltage (J–V) and the spectral response characteristics of PID-affected modules. Moreover, we focus on the degradation of the modules under positive bias. The dark J–V data are analyzed in detail by fitting to an equation based on the two-diode model [30]. We also briefly discuss possible measures to prevent the PID of the n-type rear-emitter cell modules and investigate the degradation of the modules under positive bias.

2. Experimental

Commercial n-type bifacial sc-Si solar cells composed of silver (Ag) comb-shaped electrode/SiN_x film/p^+ emitter/n-type base/n^+ back surface field/SiN_x film/Ag comb-shaped electrode were cleaved to $20 \times 20\ mm^2$-sized pieces. Interconnector ribbons were soldered onto the busbars of the front and rear Ag electrodes. The rear-emitter cell modules were fabricated by the lamination of the cells with the p^+ emitter side down. Prepared were stacks composed of conventional tempered cover glass/ethylene-vinyl acetate copolymer (EVA) encapsulant/n-type bifacial sc-Si cell with the p^+ emitter side down/EVA encapsulant/typical backsheet [poly(vinyl fluoride) (PVF)/poly(ethylene terephthalate) (PET)/PVF]. The cover glass had a size of 45 $\times 45\ mm^2$ and contained alkali metals such as Na. The modules were fabricated from the stacks in a module laminator. The lamination process mainly involves two steps: a degassing step that takes place for 5 min and an adhesion step that takes place for 15 min. The stacks were placed with the cover glass side down on a stage heated at 135 °C during lamination. The front-side configuration of the encapsulated cells is exactly the same as that of n-type Al-alloyed rear-emitter cells. The n-type rear-side emitter cell modules used herein show an energy conversion efficiency of approximately 18%.

The PID tests were performed by applying a voltage of −1000 or +1000 V to connected module interconnector ribbons with respect to an aluminum plate placed on the module cover glass in a heating chamber maintained at 85 °C. Herein, we use the terms "negative bias" and "positive bias" for biases that produce the negative and positive potentials of cells with respect to the aluminum plate, respectively. We performed the PID tests for three identical modules under each test condition. This test method and similar ones were widely used and established by many researchers as ways to easily produce PID-affected modules in a short time [17,21,28,31–40]. We use the term "PID stress" here to refer to such bias voltage and temperature stress. In this experiment, humidity in the heating chamber was not controlled during stressing; however, relative humidity in a similar setup [32] is low (approximately 2% RH). We, therefore, disregarded its influence on the performance degradation of the modules, such as the moisture ingress into the modules and the corrosion of the metal parts. Moreover, at the present state, it is unknown for how long the PID test stress corresponds to the duration that generates PID in outdoor large-scale PV systems. We used this PID test for intercomparison between the test samples.

To evaluate the degradation, J–V measurements were conducted under dark and one-sun-illuminated conditions for the modules before and after the PID tests. Saturation current densities of the first and second diodes J_{01} and J_{02}, respectively, ideality factors of the first and second diodes n_1 and n_2, respectively, parallel resistance R_p, and series resistance R_s were determined by fitting the dark J–V data to the following two-diode equation [30]:

$$J(V) = J_{01}\left[\exp\left(\frac{q(V-JR_s)}{n_1 kT}\right)-1\right] + J_{02}\left[\exp\left(\frac{q(V-JR_s)}{n_2 kT}\right)-1\right] + \frac{V-JR_s}{R_p}, \tag{1}$$

where q is the elementary charge, k the Boltzmann constant, and T the absolute temperature. J_{01}, J_{02}, R_p, and R_s were positive, n_1 was restricted to one, and n_2 was limited to greater than one. Additionally, R_s was restricted to $\geq R_{s,initial}$, where $R_{s,initial}$ is the R_s of modules before the PID tests. The two-diode fitting was performed using the statistical software Igor Pro 6 (WaveMetrics, Inc.). To estimate the spectral response losses of the degraded modules, external quantum efficiency (EQE) measurements were conducted before and after the PID tests.

3. Results

3.1. Degradation behavior under negative bias

It is so far reported that applying a high negative bias to cells leads to the degradation of many types of PV modules, such as conventional p-type c-Si modules [10–12], n-type front-emitter c-Si modules [28], n-type IBC c-Si modules [26], n-type IBC c-Si modules with front-floating emitter [27], amorphous Si (a-Si) modules [32,41], Cu(In,Ga)Se_2 cells [42] and modules [32,41], and CdTe modules [43]. Herein, we first clarify how the J–V characteristics and the EQEs of the n-type rear emitter PV modules change by applying negative bias.

Fig. 1 presents the representative one-sun-illuminated J–V curves for the n-type rear-emitter modules before and after the PID tests when applying a voltage of −1000 V to the cell with respect to the front surface of the cover glass. The modules exhibit a significant drop in V_{oc} and a relatively small drop in J_{sc}, which is consistent with the result of a previous study [29]. However, a decrease in FF is seen in this experiment, which was not observed in the previous studies [29].

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