



## New perspective on the performance stability of CdTe solar cells



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### ARTICLE INFO

#### Article history:

Received 5 June 2015

Received in revised form

29 September 2015

Accepted 7 November 2015

Available online 1 December 2015

#### Keywords:

CdTe

Solar cell

Stability

Degradation

Cu doping

Acceptor concentration

### ABSTRACT

Cu is a well-known cause for degradation of CdTe solar cells, yet, the exact mechanisms remain subject of discussion. We have chosen a novel approach to study CdTe solar cell stability by preparing CdTe solar cells in substrate configuration and applying a minimum amount of Cu to CdTe after recrystallization. These cells were exposed to an accelerated stress test. After 1000 h of operation at maximum power point under 1 sun illumination intensity at 80 °C substrate temperature such devices showed 90% of their initial power output indicating good performance stability. In order to investigate the remaining degradation and understand the role of Cu the Cu distribution in the multilayer stack was analyzed by SIMS before and after accelerated stress testing. We found that neither Cu loss in the back contact nor Cu accumulation in the CdS layer, which are often associated with degradation of CdTe solar cells, occurred in our case. C–V measurements revealed a decrease in net acceptor concentration by 70% and SCAPS simulations confirmed that this decrease can fully explain the observed performance losses of the solar cells. Time resolved photoluminescence measurements are consistent with the assumption that net acceptor loss upon stress is caused by a decay of acceptor type defects rather than by the formation of compensating donors. Acceptor loss can be explained by a redistribution of Cu inside the CdTe layer, possibly from within the grains to grain boundaries. The results demonstrate that by the use of a suitable Cu doping process that reduces Cu content at the back contact efficiency degradation due to Cu redistribution from back to front contact can be overcome. However, the observed acceptor loss appears in either configuration and seems to be independent of Cu movement from back to front or vice versa.

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### 1. Introduction

Performance stability of solar cells is an important economic and ecologic factor and has to be ensured for periods exceeding 20 years. As it is not feasible to conduct such long lasting studies, accelerated stress tests (AST) are performed in order to gain information on the performance degradation. Each laboratory uses different sets of stress parameters. Commonly used stresses include: thermal stress (up to 200 °C), light soaking (up to several 100 mW/cm<sup>2</sup> intensity), bias voltage (from a few volts reverse to a few volts forward bias), various chemical atmospheres and humidity (up to 100%). In this study we focus on internal degradation mechanisms, e.g. diffusion of elements, which occur during solar cell operation and are not caused by humidity. Therefore we chose conditions of 80 °C and illumination of 1 sun intensity while the solar cells were constantly operated at their maximum power point (MPP) in an oxygen containing but humidity free

environment (oxygen appeared necessary to avoid LED degradation). Measurements were conducted in-situ such that the stress parameters were unaltered during the time of the test.

There is a broad consensus that Cu plays a major role in performance degradation of CdTe solar cells [1–3]. However, opinions diverge on how exactly Cu affects the device stability. Finding the responsible mechanism is complicated due to the high mobility of Cu in CdTe, especially along the grain boundaries, causing Cu to be found in every layer of the solar cell even in an unstressed device [4–6]. The models on the impact of Cu on performance stability of superstrate configuration solar cells discussed in literature can be broadly divided into the following three groups, distinguished by the layer in which Cu deteriorates the electronic properties.

#### 1.1. Cu in CdS

Numerous studies report an increased concentration of Cu in the CdS and/or at the CdTe/CdS interface in solar cells stressed under various conditions [1,7–9]. Since Cu can act as a p-type dopant in CdS a proposed degradation mechanism is the compensation of CdS n-type doping and the consequential reduction of the built-in field [1,10,11]. This p-type doping is also well known

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to increase the photoconductivity of CdS leading to increased light–dark crossover in the current–voltage characteristics of the device. While there are papers stating this as detrimental for the cell [3,12], there are also others [7] confirming this effect but claiming that the photoconductivity is harmless for the performance of an illuminated device.

### 1.2. Cu at the back contact

The influence of AST on the back contact properties is strongly dependent on the back contact formation process. Therefore, it is difficult to identify a comprehensive cause for degradation. Most researchers report either a loss of Cu [1,13] or decomposition of a favorable Cu-compound (like CuTe<sub>x</sub>) [12] at the back contact. Furthermore, there are also papers ascribing the observed back contact degradation to oxidation or other non-Cu related mechanisms [7,14].

The features most often associated with degradation of the back contact are increased roll-over and series resistance after stress [7,15]. They are believed to be reflective of an increased Schottky barrier between CdTe and back contact.

### 1.3. Cu in CdTe

In literature, it is reported that the Cu concentration in CdTe is mostly unchanged during AST [7,8,16–18]. Therefore the CdTe layer is often not associated with degradation and the role of Cu in this layer is neglected. However, even if the concentration in the CdTe layer is unchanged, the migration of Cu atoms from Cd sites (acceptor states) to interstitial sites (donor states) or the grain to grain boundary diffusion of Cu can influence the performance stability. Various papers report on a decreased net acceptor concentration in CdTe after stress [2,13,19,20]. One proposed mechanism for this effect is the diffusion of excessive Cu from the back contact into the CdTe grains leading to the formation of compensating defects [19]. The decreased net doping concentration of CdTe was also used to explain the formation of a blocking back contact [20]. Further, the formation of shunt pathways through the CdTe upon excessive Cu in-diffusion is reported [21].

As all of these potential degradation mechanisms can occur simultaneously, it is desirable to develop solar cell architectures and fabrication methods, where at least some of these mechanisms can be avoided. We expect that with our substrate configuration process back to front Cu diffusion and also Cu loss at the back contact will not happen. Comparison of superstrate and substrate configuration solar cells could therefore offer a new perspective on stability issues of CdTe solar cells.

## 2. Material and methods

### 2.1. Sample preparation

First, a Mo electrical back contact layer was deposited by DC magnetron sputtering on Corning 7059 borosilicate glass (BSG) followed by evaporation of a 100 nm thick MoO<sub>x</sub> buffer layer. Then, 5–7 μm of CdTe were deposited using high vacuum evaporation at 350 °C substrate temperature followed by deposition of 400 nm CdCl<sub>2</sub> and annealing at 435 °C (25 min) in an oxygen-containing ambient. Samples were washed with water and subsequently, doping was carried out by evaporation of varying amounts (0–2 × 10<sup>16</sup> atoms per cm<sup>2</sup>) of Cu followed by annealing at 400 °C (20 min). In contrast to superstrate devices where only a fraction of Cu from a large Cu reservoir (~10 nm) is diffused at temperatures around 200 °C, in this work Cu diffusion was done at a high temperature with a small amount (0.1 nm) with the

intention to fully distribute all the Cu to CdTe and back contact. CdS was deposited by chemical bath deposition at 70 °C bath temperature. The layer stack was then treated anew with 100 nm CdCl<sub>2</sub> and a second CdS layer was applied leading to a total CdS thickness of 100–150 nm. A front contact consisting of an i-ZnO/ZnO:Al bilayer was deposited by RF magnetron sputtering. A metallic Ni/Al grid and, in selected cases, a MgF<sub>2</sub> anti-reflection coating finalized the cells. The cells with an area of 0.3 cm<sup>2</sup> were separated by mechanical scribing. Finished cells were annealed at 210 °C (10 min) followed by a fast cool down. The purity of molybdenum oxide MoO<sub>3</sub> from Alfa Aesar was 5N5. CdTe from 5N Plus Inc. was used with 6N purity and a Cu concentration < 5 ppb. CdCl<sub>2</sub> Hydrate with 4N5 purity was used. For CdS CBD cadmium acetate hydrate 4N was used with < 1 ppm Cu impurity concentration. SIMS investigation of cells without Cu addition and efficiency below 1% [22] revealed Cu concentration < 0.07 × 10<sup>14</sup> cm<sup>-2</sup> in such devices while Cu contaminated samples had up to 10% efficiency. A main contamination source turned out to be 3N purity MgF<sub>2</sub> which has been used as anti-reflective coating on some cells in the past and explains the rather good performance of some “Cu free” cells. However, the cells described in this work did not receive an MgF<sub>2</sub> coating and residual Cu content of the CdTe absorber is expected around 0.1 Å equivalents.

### 2.2. Accelerated stress testing (AST)

Accelerated stress testing was conducted in a Memmert VO 500 vacuum oven which was evacuated and refilled with dry synthetic air repeatedly to minimize moisture during stress. Light was supplied by white light LEDs from CITIZEN (type CLL 040–12 18 A1–40 3 M1 A2) with 4000 K color temperature. The intensity was adjusted to generate the same  $J_{SC}$  as for 100 mW/cm<sup>2</sup> AM1.5G illumination. This condition is referred to as “one sun illumination” in this paper. Samples were placed on a heating plate and contacted in four point probe geometry. ASTs presented in this paper were all conducted at 80 °C substrate temperature. The cells were operated at maximum power point (MPP) which was tracked using a perturb-and-observe algorithm. Current–voltage ( $J$ – $V$ ) characteristics of cells under stress were measured in-situ (at 80 °C) with an Agilent source meter at 30 min intervals.

### 2.3. Characterization methods

Ex-situ  $J$ – $V$  measurements were carried out under simulated standard testing conditions (STC) in a sun simulator before and after AST.

Capacitance–voltage ( $C$ – $V$ ) measurements were performed at room temperature in the dark with a frequency of 0.3 MHz, an oscillating voltage of 50 mV and bias voltage between –1.5 and 1.0 V. The capacitance was measured with an Agilent E4980 precision LCR meter. The width of the space charge region (SCR) at 0 V of a cell with area  $A$  was calculated assuming a plate capacitor with capacitance  $C = \epsilon_0 * \epsilon_r * A/d_{SCR}$ , and a dielectric constant  $\epsilon_r = 10$ .

Secondary ion mass spectroscopy (SIMS) profiles were measured with a time of flight (TOF-SIMS) from ION-TOF using a dual beam depth profiling. As primary ions, Bi<sup>1+</sup> with an energy of 25 keV and a current of 1 pA were employed. An area of 100 μm<sup>2</sup> was analyzed and positive secondary ions were detected. Sputtering was performed using O<sup>2+</sup> at an energy of 2 keV and a current of 400 nA on an area of 300 μm<sup>2</sup>. SIMS measurements were done with identical settings on the same machine. The SIMS Cu counts in CdTe were quantified by comparing the normalized SIMS signal (<sup>63</sup>Cu<sup>+</sup>/<sup>114</sup>Cd<sup>+</sup>) in the absorber with the normalized Cu SIMS signal of CdTe thin film on Mo/glass with a known Cu concentration. The Cu concentration in the CdTe thin film was

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