Solar Energy Materials & Solar Cells 142 (2015) 66–74

Contents lists available at ScienceDirect

Solar Energy Materials & Solar Cells

journal homepage: www.elsevier.com/locate/solmat

Process simplifications in large area hybrid silicon heterojunction solar cells

Loic Tous [a,*], Stefano Nicola Granata [a,b,c], Patrick Choulat [a], Twan Bearda [a], Alexis Michel [a], Angel Uruena [a], Emanuele Cornagliotti [a], Monica Aleman [a], Robert Gehlhaar [a], Richard Russell [a], Filip Duerinckx [a], Jozef Szlufcik [a]

[a] imec, Kapeldreef 75, 3001 Heverlee, Belgium
[b] KU Leuven, Kasteelpark Arenberg 10, 3001 Heverlee, Belgium
[c] TOTAL New Energies, 24, Cours Michelet-La Défense, 92078 Paris la défense Cedex, France

ARTICLE INFO

Article history:
Received 31 March 2015
Accepted 30 May 2015
Available online 19 June 2015

Keywords:
Crystalline silicon
Solar cell
n-Type
Hybrid
Heterojunction
Copper

ABSTRACT

Recently, large area hybrid silicon heterojunction cells (SHJ) with nickel/copper (Ni/Cu) plated front contacts were shown to benefit from a simpler processing sequence than n-PERT cells featuring a boron diffused rear emitter. Hybrid refers here to the combination of a diffused front surface field (FSF) and a SHJ rear emitter. In this work, further process simplifications for such hybrid SHJ cells are evaluated. Based on reflectance and adhesion considerations, stacks of tin-doped indium oxide and copper (ITO/Cu) and chromium/silver (Cr/Ag) are tested as alternative to the previously chosen ITO/Ag rear contact stack. Using ITO/Cu/Al as rear contact stack, average efficiencies of $20.8 \pm 0.2\%$ are presented on 6-inch wafers. We also demonstrate that the excimer laser annealing step previously employed to form nickel silicides at the front side can be skipped without comprising solder tab adhesion quality.

1. Introduction

As a large fraction of photovoltaic (PV) system costs scales with PV module efficiency, PV manufacturers are seeking ways to produce high-efficiency PV modules at a reasonable cost, mainly using solar cells based on n-type crystalline silicon (c-Si) as n-type wafers are typically of better quality than p-type counterparts [1–3]. n-Type passivated emitter and rear totally diffused (n-PERT) solar cells featuring a dopant diffusion of opposite polarity and local contacts on both sides are attracting interest because efficiencies above 20% have been reported on large area (typically 239 cm^2) using relatively simple processing sequences [3–5]. n-PERT cells can be divided into two configurations: monofacial or bifacial (i.e. contact grids on both sides), with the latter providing higher energy yields in certain conditions due to light entering both sides [4,5]. To the authors' knowledge, the best externally confirmed n-PERT cell efficiency on large area is currently 22.0% and is based on a monofacial rear-emitter design [6]. In this design (Fig. 1a), efficiencies are mainly limited by carrier recombination at both the front and rear metal contacts [7,8]. Front recombination losses can be significantly reduced by introducing a selective front surface field (FSF) formed by laser doping [8,9] or by implementing passivated contacts [10,11]. Reducing recombination losses at the rear side requires careful optimization of the rear contact fraction since reducing it to maximize open-circuit voltage (V_{oc}) and short-circuit current density (j_{sc}) comes at the expense of a lower fill factor (FF) [12–14]. A possibility to circumvent this issue is to substitute the boron-diffused rear emitter by a silicon heterojunction (SHJ) rear emitter (see Fig. 1b) consisting of intrinsic (i) and boron doped (p^+) hydrogenated amorphous silicon layers (a-Si:H) and to contact this SHJ rear emitter using blanket layers [15–17]. This way, current flow at the rear side is vertical (1-dimensional) which simplifies junction and contact optimization [16]. In addition, a front side masking step is no longer required during a-Si:H(i/p^+) deposition by Plasma Enhanced Chemical Vapor Deposition (PECVD) which is a single-side emitter formation process unlike high temperature gas phase diffusion. Furthermore, rear side polishing can be skipped since very low SHJ emitter recombination currents have been demonstrated on textured surfaces [19]. Compared to conventional SHJ solar cells featuring a-Si:H layers on both sides, this design – hereafter referred to as hybrid SHJ – is limited by carrier recombination under the front contacts but presents the advantage that parasitic absorption in the front a-Si:H and transparent conductive oxide (TCO) layers in not an issue thus allowing higher j_{sc} values [20]. Using this

* Corresponding author. Tel.: +32 32 16 287 522.
E-mail address: loic.tous@imec.be (L. Tous).

http://dx.doi.org/10.1016/j.solmat.2015.05.049
0927-0248/

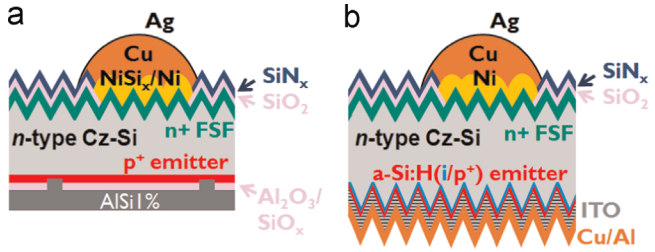

Fig. 1. (a) Schematic representation of a monofacial rear-emitter n-type passivated emitter and rear totally diffused (n-PERT) cell as described in Ref. [14]. (b) Schematic representation of a hybrid silicon heterojunction (SHJ) n-type solar cell as fabricated and investigated in this work.

hybrid SHJ design in combination with self-aligned Ni/Cu/Ag plated front contacts, efficiencies up to 20.1% were reported on large area using commercially-available n-type Czochralski (n-Cz) grown wafers [17]. However, a relatively complex single-side excimer laser annealing (ELA) step had to be employed after Ni plating to form nickel silicides ($NiSi_x$) under the front side contacts since conventional rapid thermal annealing (RTA) in the range of 250–450 °C was shown to degrade the SHJ rear emitter properties. Instead, it would be simpler and more cost-effective if the $NiSi_x$ formation step could be skipped without compromising efficiency and adhesion quality. This is demonstrated in this work by fabricating hybrid SHJ solar cells on $15.6 \times 15.6\ cm^2$ n-Cz wafers and comparing efficiency and solder tab adhesion results to previously reported data [17]. In the first part of this paper, we also evaluate various rear contact layers for hybrid SHJ cells.

2. Experimental

2.1. Rear contact test structures

Various test structures were prepared to evaluate rear contact layers for hybrid SHJ cells based on internal rear reflectance, adhesion, and thermal stability. In a monofacial SHJ design, omitting the transparent conductive oxide at the rear side limits the choice of rear metals to a few candidates to keep optical losses to a minimum [16–21]. Based on weighted reflectance measurements in the 1000–1200 nm range and effective lifetime measurements, Bivour et al. [16] concluded that Ag was the most suited contact metal among the following set of thermally evaporated metals: Cr, Ti, Pd, Al, Cu, Au, and Ag. This is because Au, Pd, Cu, and Al were shown to severely degrade SHJ emitter properties after annealing at 200 °C while Ti and Cr were found to lead to poor rear side reflection. However, these results were obtained on double-side shiny-etched wafers which might lead to misleading results since parasitic absorption by surface-plasmons has been shown to be more severe on rough surfaces with Ag than with Al [22]. In addition, evaporated Ag has been reported to result in insufficient adhesion on silicon surfaces [23]. Furthermore, hybrid SHJ solar cells fabricated in this work feature Ni/Cu/Ag plated front side contacts that were obtained using an inline tool in which wafers are fully immersed in plating electrolytes. This raises concerns that front side Ni/Cu/Ag plating might weaken or even destroy rear side adhesion due to electro-chemical effects.

The first set of test structures (see Fig. 2a) was prepared on chemically polished ("polish") and random pyramid textured ("randtex") wafers to determine the optimum rear contact layers for hybrid SHJ cells based on reflectance and adhesion before- and after-Ni/Cu/Ag plating. For this, six-inch semi-square ($239\ cm^2$) n-type Cz-Si wafers were saw damage removed (SDR) and randtex on both sides using KOH-based solutions. Following this, one group of wafers received an additional rear-polishing step in an

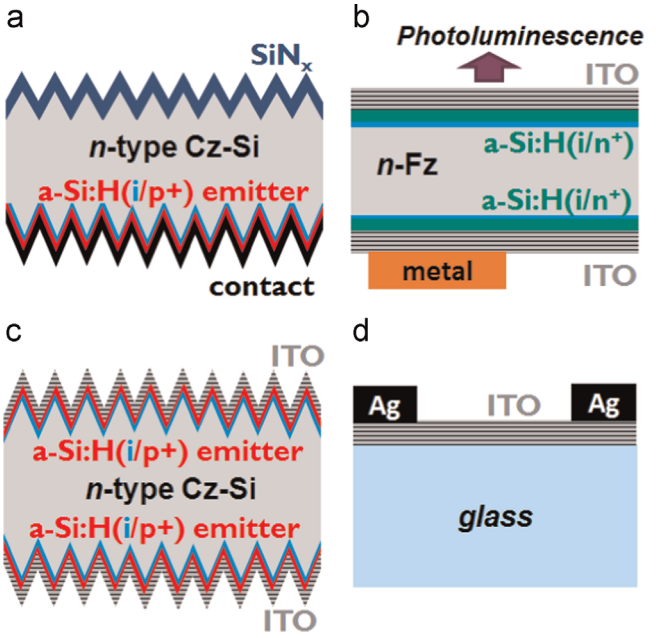

Fig. 2. (a)–(d) Schematics of the various rear contact structures prepared, see text for details.

inline tool which removed ~12 μm of Si. Subsequently, all wafers received at the front side a silicon nitride (SiN_x) anti-reflective coating (ARC) deposited by direct PECVD. Front surface field (FSF) formation was omitted so that free carrier absorption in the FSF would not affect reflectance measurements. Intrinsic and doped a-Si:H(i/p$^+$) layers, forming the SHJ rear emitter, were deposited at the rear side by PECVD (AK1000, Roth & Rau; parallel-plate reactor operated at 13.56 MHz). Thicknesses were ~4 nm and ~12 nm respectively. More details regarding the a-Si:H depositions can be found elsewhere [24]. Afterwards, various rear contact layers were deposited either by direct current (DC) sputtering (ITO, Cu, Ti) or by thermal evaporation (Ag, Cr, Al, Pd). More details regarding optimization of the ITO layer can be found elsewhere [25]. This resulted in the following set of rear contact layers: Cr, Pd, Al, Ag, Cr/Ag, ITO, ITO/Cu, ITO/Ti/Cu, and ITO/Ag. All layers were ~150 nm thick (meaning ITO/Cu was ~300 nm thick in total) except for the Cr/Ag and the ITO/Ti/Cu stacks. For the Cr/Ag stack, only ~1 nm of Cr was deposited in an attempt to improve adhesion without reducing rear side reflection. For the ITO/Ti/Cu stack, a thickness of ~30 nm of Ti was chosen as Cu diffusion barrier based on recipes developed at imec for integrated circuits. Finally, samples were annealed successively for 5 min under N_2 in a rapid thermal annealing (RTA) tool (AccuThermo AW410, Allwin21 Corp., Morgan Hill, USA) at temperatures in the range of 150–250 °C. For each annealing temperature, reflectance curves were measured from the front side in the range of 1000–1400 nm using a spectral response setup (PVE300, Bentham instruments Ltd., Reading, UK; $4\ mm^2$ spot size). Scotch tape tests were conducted on a set of samples that was annealed at 150 °C, to quickly evaluate adhesion before and after front side Ni/Cu/Ag plating. The front side Ni/Cu/Ag plating sequence consisted in native oxide removal, bias-assisted light-induced plating of Ni and Cu (thin seed layer), Cu electroplating (~8–12 μm), Ag capping (~150 nm) by immersion plating, and finally drying and unloading [26]. Scotch tape was applied on the rear side of the samples by hand, manually pulled at 90° angle, and the pieces of tape were visually inspected for metal residues.

Some of the hybrid SHJ cells fabricated in this work feature Cu contacts on both sides and contact annealing is performed at temperatures up to 250 °C. Cu diffusion in silicon can be significant