Solar Energy Materials & Solar Cells 137 (2015) 193–201

Contents lists available at ScienceDirect

Solar Energy Materials & Solar Cells

journal homepage: www.elsevier.com/locate/solmat

0.4% absolute efficiency increase for inline-diffused screen-printed multicrystalline silicon wafer solar cells by non-acidic deep emitter etch-back

Prabir Kanti Basu [a,*], Felix Law [a], Shanmugam Vinodh [a,b], Avishek Kumar [a], Paul Richter [c], Frank Bottari [c], Bram Hoex [a]

[a] Solar Energy Research Institute of Singapore, National University of Singapore, 7 Engineering Drive 1, Block E3A, 06-01, Singapore 117574, Singapore
[b] Department of Electrical and Computer Engineering, National University of Singapore, 7 Engineering Drive 1, Block E3A, 06-01, Singapore 117574, Singapore
[c] BTU International, Inc. 23 Esquire Road, North Billerica, MA 01862, USA

ARTICLE INFO

Article history:
Received 14 August 2014
Received in revised form
5 January 2015
Accepted 9 February 2015
Available online 5 March 2015

Keywords:
Industrial multicrystalline silicon wafer solar cells
Inline diffusion
SERIS etch
HF-free and non-acidic etch-back solution
Heavy emitter etch-back

ABSTRACT

Emitter formation is one of the most critical and crucial process steps in the fabrication of standard silicon wafer solar cells. Typically the photovoltaic industry uses tube based phosphorus diffusion, using phosphorus oxychloride as the dopant source. Alternately, a low-cost inline diffusion using phosphoric acid as a dopant source can be used. However, proper process conditions must be used to meet solar cell energy conversion efficiencies obtained by tube diffusion. In this work, we present the application of a non-acidic homogeneous emitter etch-back process – the 'SERIS etch' – for inline-diffused emitters in order to raise the efficiency of multicrystalline silicon (multi-Si) wafer solar cells. We apply both light and heavy emitter etch-backs on inline-diffused emitters with sheet resistance (R_{sq}) values in the 40–60 Ω/sq range to achieve emitters with a target R_{sq} of ~70 Ω/sq. The emitter surface reflectance and doping uniformity are maintained even after an etch-back that results in a R_{sq} change of ~30 Ω/sq. An average cell efficiency gain of 0.4% (absolute) is reported for cells with heavy etch-back when compared to the as-diffused non-etch-back screen-printed full-area aluminum back surface field solar cells and efficiencies up to 17.9% are achieved. Besides, best lot of the etch-back inline-diffused cells shows a 0.2% (absolute) efficiency gain over the standard tube-diffused cells. These results show that the 'SERIS etch' etch-back process can enable higher-efficiency industrial inline-diffused multi-Si wafer solar cells.

1. Introduction

Crystalline silicon (Si) wafer solar cells currently dominate the global photovoltaic (PV) market. Among the silicon wafer solar cells, solar cells fabricated using multicrystalline silicon (multi-Si) wafers dominate over solar cells produced using monocrystalline silicon (mono-Si) despite their typically lower energy conversion efficiencies. This is explained by the fact that multi-Si wafers can be produced at significantly lower costs compared to their mono-Si counterparts [1]. Increasing the conversion efficiency of multi-Si wafer solar cells in a cost-effective way is a key area of research in the PV field. The emitter formation process is one of the areas where significant cost reduction is still possible. The current state-of-the-art industrial technology is tube diffusion, with its confirmed high quality and repeatability in junction formation. It uses high-purity phosphorus oxychloride ($POCl_3$) as a phosphorus (P) dopant source resulting in high-efficiency Si wafer solar cells. The downsides of tube diffusion are a relatively high capital cost and the fact that the process is batch-based, therefore requiring complex and costly wafer handling.

An alternative approach for emitter formation is inline diffusion. Inline diffusion uses conventional belt furnaces with phosphoric acid (H_3PO_4) as P source and the process is significantly less expensive than tube diffusion. As inline diffusion directly deposits the dopant source on the wafer surface, it typically achieves a better doping homogeneity compared to tube diffusion, especially for emitters with a high sheet resistance. However, the usage of an open-ended furnace, lower-grade chemical precursors, metal conveyor belts and shorter process times have their own adverse impacts on the solar cell efficiency. As a result, processing conditions must be chosen to address these impacts, otherwise typical cell efficiency of an inline-diffused emitter (ILDE) Si solar cells can be lower compared to their tube-diffused counterpart. A surface 'dead layer' can be formed on the ILDE surface by a high dopant concentration at the surface and surface contaminants resulting from direct deposition of dopants on the wafers [2,3]. This dead

* Corresponding author. Tel.: +65 6601 1739; fax: +65 6775 1943.
E-mail address: prabir.basu@nus.edu.sg (P.K. Basu).

http://dx.doi.org/10.1016/j.solmat.2015.02.004
0927-0248/

layer directly limits short-circuit current (I_{sc}) and open-circuit voltage (V_{oc}) of the solar cell [3–5]. Also the short duration of the diffusion process affords less impurity gettering and this can limit the V_{oc} and efficiency of ILDE solar cells [6,7]. A practical way to minimize these efficiency constraints is to coat both sides of the Si wafer with phosphorus dopant. This minimizes back surface contamination from the metallic conveyor belt [8] and enhances P gettering [6]. In addition, it has been reported that after phosphosilicate glass (PSG) layer removal by dilute hydrofluoric (HF) acid solution, rod-like structures of silicon phosphide (SiP) precipitates are still observed on the emitter surfaces [9]. These SiP rods are attributed to the presence of high P concentrations above the solid solubility limit and rapid cooling of the dopant solution (H_3PO_4 and solvent) at the end of diffusion process [9]. These structures are also part of the dead layer associated with inline-diffusion process. Thus the success in achieving high PV efficiencies using inline diffusion lies in reduction or even the complete removal of the dead layer.

Several research groups have applied different surface etching or cleaning processes to remove the dead layer (along with SiP precipitates) [3,7,8,10–13] and these 'cleaning' or 'etching' processes for the emitters are commonly known as emitter etch-back processes. A surface treatment by the solution of nitric acid (HNO_3) and HF was used on an ILDE surface by Voyer et al. [10] on mono-Si wafers. With the 'ECN Clean' etch-back process Hoornstra et al. [8] reported efficiencies up to 16% for ILDE multi-Si wafer solar cells. Later Stassen et al. [11] confirmed partial removal of 'non-active phosphor', which in turn reduces number of recombination centers for multi-Si wafers, by using the so-called 'BakerClean PV-160®' etch-back solution. An absolute efficiency gain of 0.2–0.3% with a moderate increase in emitter R_{sq} (i.e., ΔR_{sq}) of 6 Ω/sq was reported when using this 'surface clean' [11]. Ebong et al. [3] reported an 'extended surface clean' process and achieved an average efficiency of 17.4% for ILDE mono-Si wafer cells. Using an inline diffusion furnace with ceramic rollers and 'augmented clean' emitter etch-back process, Rousenville et al. [12] reported a champion efficiency of 18.2% for mono-Si solar cells featuring a plated Ag front metallization (using a screen-printed Ag seed layer). However, the most widely industrially used etch-back technology was developed at the University of Konstanz and uses a cold ($<$ 10 °C) mixture of HF and HNO_3 for to etch back the emitter [13]. This process has also been used extensively in formation of selective-emitter solar cells [14–17]. All the processes mentioned up to now only enable relatively shallow homogeneous emitter etch-backs of up to 10 Ω/sq. The main problem associated with deeper etch-backs is that they are typically not very conformal and thus reflectance from the emitter surface increases after a deeper etch-back [18]. Consequently the potential of the etch-back processes is limited.

Recently, Basu et al. [7,19,and20] introduced a new, non-acidic, HF-free and uniform emitter etch-back process, the so-called SERIS etch. The 'SERIS etch' was successfully applied on IDLE mono-Si wafer solar cells with etch-backs in the range of ΔR_{sq} ~25 Ω/sq and achieved efficiencies up to 18.7% and 19.0%, respectively, for full-area aluminum back surface field (BSF) [7] and local aluminum back surface field (Al-LBSF) [19] silicon wafer solar cells.

In this paper, we report on the first application of the 'SERIS etch' on ILDE multi-Si solar cells. Etch-backs up to ΔR_{sq} ~30 Ω/sq while maintaining the front surface morphology and R_{sq} uniformity is reported; and the dead layer was confirmed to be completely removed. Compared with as-diffused ILDE cells, a 0.4% (absolute) efficiency gain was demonstrated for the heaviest etch-back emitter with R_{sq} ~70 Ω/sq.

Table 1
Target and measured sheet resistance values for all the inline and tube-diffused emitters with their average and standard deviation (SD) values. For the inline emitters both the as-diffused and etched-back parameters are indicated. The only process parameter changed during the inline diffusion process was the peak diffusion temperature, while the emitter etch back time was changed in order to achieve a ~70 Ω/sq emitter after the etch-back process.

Emitter groups	As-diffused emitters				Etch-back emitters		
	Peak diffusion temperature (°C)	Targeted R_{sq} (Ω/sq)	Measurement R_{sq} (Ω/sq)		Achieved R_{sq} (Ω/sq)		Etch-back duration (s)
			Average	SD	Average	SD	
Group 1	845	70	70.3	2.9	—	—	—
Group 2	855	60	61.2	2.9	67.0	3.1	30
Group 3	870	50	49.9	1.6	65.3	2.6	80
Group 4	880	40	41.8	1.3	68.0	2.9	150
Group 5	840	70	67.8	2.6	—	—	—

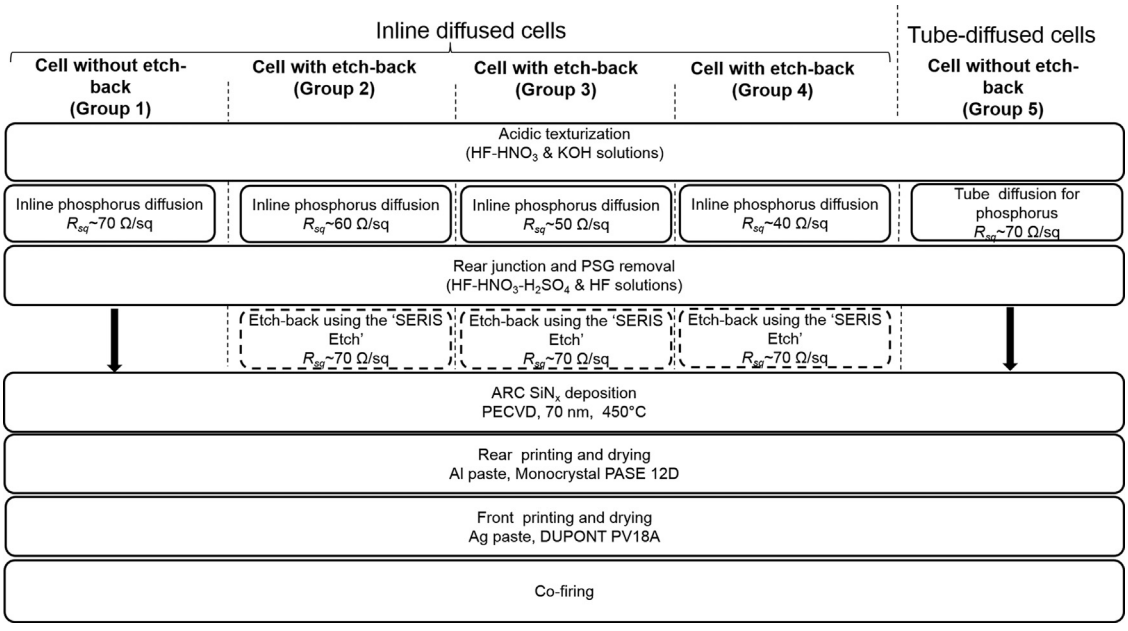

Fig. 1. Fabrication process flow for the ILDE (without or with etch-back) and tube-diffused solar cells. The modified etch-back recipes using the 'SERIS etch' are shown in the dashed boxes.