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Electrical properties of the rear contact structure of MWT silicon solar cells

Elmar Lohmüller *, Mikaella Thanasa, Benjamin Thaidigsmann, Florian Clement, Daniel Biro

Fraunhofer Institute for Solar Energy Systems (ISE), Heidenhofstraße 2, 79110 Freiburg, Germany

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ABSTRACT

In certain metal wrap through (MWT) solar cell structures, the external rear contact – that is connected to the front grid by the via contacts – directly overlaps the silicon base with opposite polarity. Since no intermediate p–n-junction is present in-between, leakage currents under forward bias may occur. Such leakage currents directly affect the conversion efficiency of the cell. This work investigates the electrical contact properties of five screen printing via pastes to p-type and n-type Czochralski-grown silicon with different surface topographies and different intermediate dielectric insulation layer systems. Dark current–voltage (*IV*) measurements on test structures reveal a significant impact of the via paste on the *IV* characteristics. In addition, especially for n-type silicon, reverse bias load leads to significantly increased forward leakage currents. Stability tests performed with p-type MWT solar cells (either with aluminum back surface field or passivated rear surface) reveal no significant fill factor drops when appropriate via pastes are used.

1. Introduction

Many highly efficient metal wrap through (MWT) [1] solar cell types based on monocrystalline p-type or n-type silicon as base material with conversion efficiencies of about 20% or even higher have been reported [2–6].

Typically, the external rear contacts and the vias are metallized simultaneously with a non-fire-through silver screen printing paste, called "via paste". The term "non-fire-through" refers to the property of the paste not to penetrate silicon nitride (SiN_x) layers.

A major challenge in the fabrication of MWT solar cells is the use of a suitable via paste depending on the cell structure. A reliable and continuous via metallization is essential in terms of low series resistance contribution for achieving high fill factors [7]. For conventional p-type silicon MWT cell structures with aluminum back surface field (MWT-BSF, Fig. 1a) or passivated emitter and rear (MWT-PERC [8], Fig. 1c), the presence of an emitter in the vias and on the rear ensures the electrical contact separation between via paste (n-type contact) and p-type silicon base. For this application, via pastes have been optimized with respect to low shunting behavior [8–10].

Recently presented p-type MWT cells feature a simplified structure enabling the use of more cost-effective fabrication process sequences. No emitter is present in the via and on the rear for the p-type MWT-BSF+ cell [5] illustrated in Fig. 1b, while for the p-type high-performance MWT (HIP-MWT) approach [11], shown in Fig. 1d, only the rear emitter is omitted. For both MWT cell structures the via paste itself – either in direct contact with the silicon base as for the MWT-BSF+ or with an intermediate dielectric as for the HIP-MWT cell structure – must not form an electrically conductive contact to the adjacent silicon base. In forward bias, i.e. normal operation mode, up to the open-circuit voltage no significant leakage current should occur to prevent fill factor and open-circuit voltage losses.

Two recently presented MWT cell structures using n-type silicon as base material are depicted in Figs. 1e and f [12]. The front passivation layer stack consists of aluminum oxide or silicon oxide and silicon nitride, whereas the rear passivation is commonly realized with silicon nitride. Both n-type MWT cells have an emitter neither on the rear side nor inside the vias but feature differently structured phosphorus-doped BSFs. Again, the via paste must not form an electrically conductive contact to the silicon.

As the preceding discussion of the different MWT cell structures shows, solely the non-fire-through property of the via pastes is no longer sufficient. In addition, the via pastes themselves have to prevent electrical contact formation when applied directly onto silicon with the same polarity, whether with or without intermediate dielectric. Hence, for the latest MWT cell structures a suitable via paste must meet both requirements.

* Corresponding author. Tel.: +49 761 4588 5701.
E-mail address: elmar.lohmueller@ise.fraunhofer.de (E. Lohmüller).

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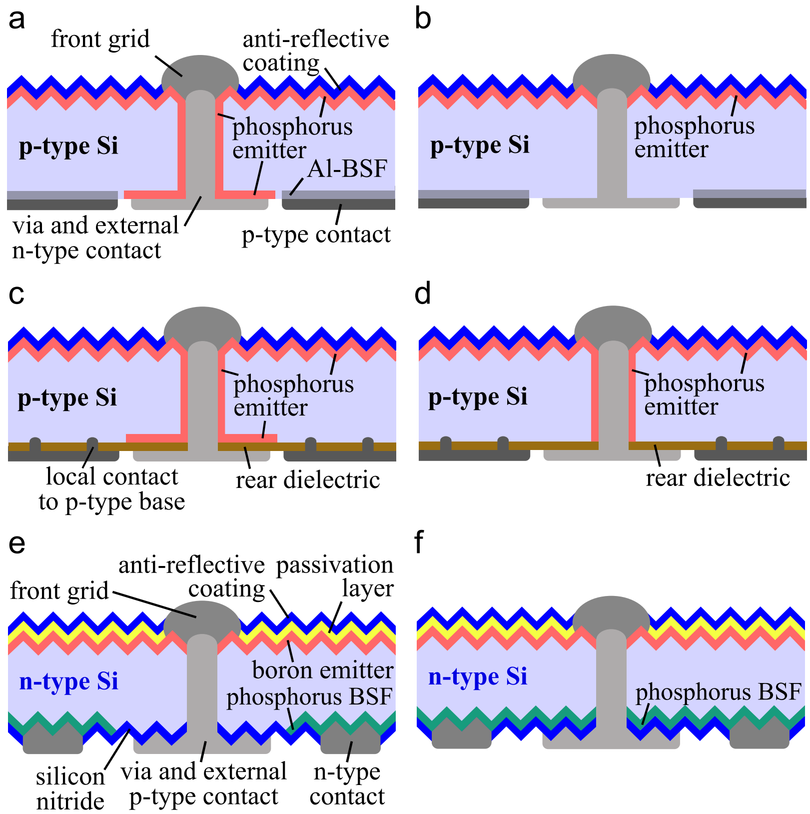

Fig. 1. (a) MWT-BSF, (b) MWT-BSF+, (c) MWT-PERC, (d) HIP-MWT, (e) nMWT-1 and (f) nMWT-2. Schematic cross sections of six different MWT solar cell structures. (a, c) Conventional p-type silicon MWT structures with via and rear emitter. (b) The p-type MWT-BSF+ structure denotes a simplified MWT-BSF structure without emitter in the via and on the rear. (d) The p-type HIP-MWT approach is a MWT-PERC structure without rear emitter. (e) The nMWT-1 structure shows an n-type MWT solar cell with structured rear phosphorus-doped BSF. (f) The nMWT-2 structure instead features a full-area phosphorus-doped BSF.

Since partial shading of a photovoltaic module can lead to reverse bias condition for the shaded cells, reverse breakdown and possible hot spot formation also have to be addressed [13]. Therefore, the performance of the via pastes in reverse bias condition is of interest. MWT solar cells enabling sufficiently low reverse breakdown voltages can, however, represent an integrated bypass diode approach allowing a controlled reverse current flow with less external bypass diodes in the module [14].

Some work has already been done regarding the electrical contact properties between screen-printed via pastes and Czochralski-grown silicon (Cz-Si). For p-type HIP-MWT cells both forward and reverse bias behavior can be modified by different intermediate rear dielectrics [4,14,15] or the use of different via pastes [4]. For the p-type MWT-BSF+ approach, our previously investigated via pastes showed too high leakage currents and were not suitable for this cell concept [4]. Nevertheless, Yin et al. [5] achieved conversion efficiencies up to 19.6% for such MWT-BSF+ cells demonstrating the availability of a via paste which can be directly applied onto the subjacent silicon base.

First investigations regarding the electrical contact property between via pastes and n-type Cz-Si revealed rather high leakage currents [4].

In the present work, five via pastes from three paste manufacturers[1] and one standard fire-through reference silver paste – commonly used for the front metallization of p-type solar cells – are investigated on n-type and p-type Cz-Si test structures. Since the occurring forward leakage currents increased after reverse bias load in previous experiments [4,14], the influence of reverse bias load is investigated in more detail. Furthermore, some of the via pastes are also tested on p-type Cz-Si MWT-BSF+ and p-type Cz-Si HIP-MWT solar cells.

2. Screen-printed silver-insulator-semiconductor contacts

For screen-printed and fired front silver contacts commonly applied for p-type silicon solar cells, the actual mechanisms of contact formation to the highly doped n-type emitter and of current transport are still being discussed [16–18]. Tunneling through a thin dielectric layer is assumed to be one of the major current transport mechanisms [14,16,19,20] leading to ohmic contact properties [21].

In contrast, the design of the via pastes used for MWT cells should be such, that no ohmic contact to silicon is formed. The contact system investigated in this work consists of a screen-printed and fired via paste with silver as conductive component, an intermediate dielectric and the silicon wafer. One model to describe the electrical characteristics of such a contact system is given by quantum mechanical tunneling of charge carriers through the intermediate dielectric layer [14,22].

Nonlinear current–voltage (*IV*) characteristics have been observed on lightly doped p-type as well as n-type silicon for screen-printed contacts realized with silver via pastes [4,14,15].

In a previous study [14], we investigated these nonlinear *IV* characteristics of such a silver via paste on lightly doped p-type Cz-Si with and without intermediate dielectric layers in more detail and concluded that the dominating current transport mechanism is quantum mechanical tunneling through the dielectric between silver contact and silicon. Despite the fact that via pastes are designed not to penetrate SiN_x layers, samples with intermediate dielectric (SiN_x layer thickness of at least 50 nm, thus

[1] The via pastes were provided by DuPont Microcircuit Materials (contact person: Russell Anderson, e-mail: russell.anderson@dupont.com), Heraeus Precious Metals (Matthias Hoerteis, matthias.hoerteis@heraeus.com), and Murata (Uwe Mirschberger, uwemirschberger@murata.com).