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Recombination behavior and contact resistance of n^+ and p^+ poly-crystalline Si/mono-crystalline Si junctions

Udo Römer [a,*], Robby Peibst [a], Tobias Ohrdes [a], Bianca Lim [a], Jan Krügener [b], Eberhard Bugiel [b], Tobias Wietler [b], Rolf Brendel [a]

[a] Institute for Solar Energy Research Hamelin (ISFH), Am Ohrberg 1, D-31860 Emmerthal, Germany
[b] Institute of Electronic Materials and Devices, Leibniz Universität Hannover, Schneiderberg 32, D-30167 Hannover, Germany

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ABSTRACT

We present an investigation of the electrical characteristics – recombination and contact resistance – of poly-crystalline (poly) Si/mono-crystalline (*c*) Si junctions and of the influence of the interfacial oxide between the poly-Si and the *c*-Si on these characteristics. In particular, we compare thermally grown oxides with different thickness values with wet chemically grown oxides. Both n- and p-type poly-Si emitters are investigated. For one combination (n-type poly-Si, thermal oxide), we compare planar and textured surfaces.

For all oxide types investigated, we achieve combinations of low recombination current densities <20 fA/cm² and low specific contact resistances $<0.1\ \Omega\,\text{cm}^2$. The corresponding implied open-circuit voltages measured on our test structures are 732 mV (n-type poly-Si) and 711 mV (p-type poly-Si). By applying these poly-Si layers on a solar cell structure, we achieve an open-circuit voltage of 714 mV and a series resistance of $0.6\ \Omega\,\text{cm}^2$.

1. Introduction

While the price of photovoltaic modules has been decreasing strongly over the past years, the balance of system costs remain more or less stable [1]. Therefore, one approach for a further reduction of the costs per watt peak is the increase of the power conversion efficiency. Since the recombination losses in the passivated cell regions have been reduced in passivated emitter and rear solar cells (PERC) with local Al rear contacts [2,3] and in n-type passivated emitter and rear totally diffused (PERT) solar cells [4,5], one of the major remaining recombination loss mechanisms in these type of cells is the recombination at the metal contacts. To minimize these losses the contact area may be reduced further. However, there is a certain lower limit for the contact area of a few percent of the total cell area. By decreasing it further, the specific contact resistance of metal/silicon junctions of several $\text{m}\Omega\,\text{cm}^2$ would imply significant resistive losses. An alternative approach is the use of junctions which selectively block one carrier type while efficiently transporting the other carrier type and thus strongly reduce recombination at the metal/semiconductor interface on top of such a junction. A prominent example of such a "carrier selective junction" are hetero-junctions between amorphous (a) Si with a band gap of ~1.7 eV and mono-crystalline (c) Si with a band gap of 1.12 eV. The "selective blocking effect" in *a*-Si/*c*-Si hetero-junctions is implied by the valence and conduction band offsets. With this approach, excellent open circuit voltages up to 750 mV and efficiencies up to 24.7% have been reported [6]. Nevertheless, the restriction to low temperatures when processing *a*-Si/*c*-Si hetero-junction cells implies technical issues. For example, the optical and electrical properties of the transparent conductive oxide (TCO) could be improved by high temperature processing. A promising, temperature-stable alternative for "carrier selective junctions" are poly-crystalline silicon (poly-Si) emitters, which are deposited on an interfacial oxide grown on a mono-crystalline Si base. These types of junctions are already applied in state-of-the-art bipolar transistors to reduce the injection of charge carriers from the base into the emitter without reducing the injection from the emitter into the base [7–9]. For solar cell applications, this corresponds to a reduction of the emitter saturation current density (J_{0e}) without a significant increase in the series resistance. This has nicely been shown by Gan and Swanson [10], who reported J_{0e} values less than 20 fA/cm² and "contact resistances" of less than $0.1\ \text{m}\Omega\,\text{cm}^2$ for both n-type poly-Si and p-type poly-Si emitters.

The results of Gan and Swanson [10] had been obtained on samples featuring a thin (<2 nm) thermally grown interfacial oxide between the poly-Si and the *c*-Si. The junctions were formed within a "two-step" approach: the poly-Si deposited without in situ doping

* Corresponding author. Tel.: +49 5151 999643; fax: +49 5151 999400.
E-mail address: roemer@isfh.de (U. Römer).

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was first annealed in a high temperature step, while the dopant diffusion process was applied as a second step. Gan and Swanson found the temperature and duration of the first annealing step to be crucial for the contact resistance of the junction. This was explained with a breaking-up of the interface oxide upon annealing, as observed in transmission electron microscopy (TEM) measurements [11,12]. Gan and Swanson [10] considered the current transport across the junction to be dominated by the current flow through these pinholes in the oxide rather than by tunneling. This picture is supported by a model recently proposed by Peibst et al. [13]. Recently, very promising results have been shown on solar cells featuring an n-type poly-Si/n-type *c*-Si base contact and a "standard" p-type *c*-Si emitter [14,15].

While the understanding of the physical mechanism mediating the current transport across the interfacial oxide might still require further research, it has become obvious in all previous works that the properties of the interfacial oxide are crucial for the electrical characteristics of poly-Si/*c*-Si junctions. For application of the poly-Si emitter concept in photovoltaics, it would be desirable to reduce process complexity by substituting the thermal oxidation [10] by a simpler interfacial oxide growth method, e.g. by wet chemical oxidation in a cleaning sequence which is anyhow applied in a solar cell fabrication process. Furthermore, for double-side contacted solar cells, excellent poly-Si/*c*-Si junction characteristics on textured surfaces are required.

Therefore, we study in this paper the influence of the interfacial oxide on the electrical characteristics – recombination and contact resistance – of poly-Si/*c*-Si junctions. Both n- and p-type poly-Si emitters are investigated. We compare wet chemically grown and thermally grown oxides on planar surfaces and the latter also on textured surfaces. We will show that the electrical properties of the poly-Si/*c*-Si junctions strongly depend on the post-deposition thermal treatment, which has to be optimized for each interfacial oxide. For a fast and non-destructive determination of an upper limit of the resistance of the poly-Si/*c*-Si junctions, we present a new measurement method. In order to verify on cell level the promising implied open circuit voltages and low interface resistances measured on test structures, we investigate solar cell structures with p-type poly-Si emitter and n-type poly-Si back surface field.

2. Sample preparation

2.1. J_0 test structures

We use saw-damage etched n-type Czochralski silicon wafers with a resistivity of 8–9 Ω cm and a thickness of 160 μm as substrate material. These substrates are oxidized in a wet chemical bath or in a tube furnace. The bath consists in one case of a standard cleaning solution containing HCl and H_2O_2 and in the other case of a HNO_3 solution. The resulting thickness of these oxides is for both solutions determined to 1.4 nm by ellipsometry and TEM measurements. The thermal oxides are fabricated with different processes resulting in oxide thicknesses of 2.4 nm to 3.6 nm. Subsequently, 100–200 nm thick layers of undoped amorphous silicon are deposited on top of the oxide by low pressure chemical vapor deposition (LPCVD). Next, we apply a high temperature annealing step in a nitrogen atmosphere for the oxide break-up. The plateau temperature and the corresponding process durations are varied. Afterwards, a $POCl_3$ – (for n-type poly-Si emitters) or BBr_3 – (for p-type poly-Si emitters) diffusion step is applied. After forming gas annealing (FGA) we measure the saturation current density (J_0) of the poly-Si layers with a WCT-120 lifetime tester (Sinton Instruments) and the method of Kane and Swanson [16]. A schematic drawing of the J_0 test structures can be seen in Fig. 2.

2.2. Solar cells

For the demonstration of the applicability of the poly-Si/*c*-Si junctions on solar cells, we produce proof-of-principle solar cell devices. The aim of this cell run is not the demonstration of highest efficiencies, but to show the high V_{oc} potential of the poly-Si/*c*-Si junctions without a drawback in the series resistance.

The solar cells are fabricated using the same wafer material as for the test structures. These (planar) wafers are oxidized with a 2.4 nm thick thermal oxide and a layer of intrinsic LPCVD poly-Si is deposited on top of the oxide. The samples are then annealed for 30 min at 1050 °C in an inert atmosphere. The doping of the rear poly-Si layers is conducted by depositing a plasma enhanced chemical vapor deposited (PECVD) silicon nitride (SiN_x) as protection layer on the front side of the samples, applying a BBr_3-diffusion step and removing the nitride layer in an HF-solution. The front side doping is conducted similarly, by depositing a SiN_x protection layer on the rear side, applying a $POCl_3$-diffusion step and again removing the nitride layer with HF. After a FGA step the samples are cut into 2.5×2.5 cm² pieces with a nanosecond laser. Then an Indium Tin Oxide (ITO) layer is deposited by sputtering on the rear and front side of the pieces through a mask with 2.1×2.1 cm² large openings. Metallization is done by evaporating a 2×2 cm² large Al pad on the rear side and an Al finger grid on the front side. We measure the implied *JV*-curve with the WCT-120 lifetime tester after the FGA step (before cutting) and after ITO deposition. After metallization we measure light *IV*- and $J_{sc}V_{oc}$-curves with and without a shadow mask with a 2.06×2.06 cm² large opening.

3. Structural investigations

To check our picture that the "oxide break-up step" indeed induces the formation of oxide pinholes with an areal density which is increasing for increasing thermal budgets, we performed structural investigations of our samples using transmission electron microscopy (TEM). While this technique enables very high resolutions in the sub-nanometer range, the sample area which can be screened for oxide pinholes is also limited to a few hundred nanometers. Thus, it is challenging to resolve pinholes with an areal density of $\sim 10^7$ cm^{-2} (corresponding to an average pinhole-to-pinhole distance of ~3 μm) by TEM. Unfortunately, this is the order of magnitude for the oxide pinhole density in our samples (with low J_0 but already acceptably low interface contact resistance ρ_{int}) we would expect from our model [13]. Thus, we choose a sample with a thin wet chemically grown oxide in a HNO_3 bath which received a very extensive oxide break-up step (30 min @ 1050 °C) for TEM investigations. This sample already shows a quite high recombination current of 508 fA/cm^2 (see below), but was expected also to exhibit the highest pinhole area density and the largest pinhole diameter.

Indeed, numerous locations with a non-continuous interfacial oxide can be resolved (Fig. 1a)). The Si crystallites above the broken up regions are re-oriented according to the crystal orientation of the substrate (Fig. 1b)). We expect that the pinhole diameter in samples with moderate thermal budget is smaller (similar to the observation of Wolstenholme et al. [11]).

4. Contact resistance estimation on non-metalized samples

4.1. Four point probe measurements

For the purpose of a fast and non-destructive estimation of the interface contact resistance of isotype junctions (in this paper n^+ poly-Si/*n* *c*-Si/n^+ poly-Si), we carry out Four Point Probe (4PP)