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## Silicon nanocrystals in carbide matrix

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## ABSTRACT

Ordered silicon nanocrystals in silicon carbide are produced by Plasma Enhanced Chemical Vapor Deposition by means of the multilayer approach followed by annealing at 1100 °C. The crystallization is verified by Raman scattering, X-ray diffraction, Transmission Electron Microscopy, and UV–vis spectroscopy. The conditions for the periodic structure to survive the high temperature annealing and for the SiC barrier to confine the Si crystal growth are examined by energy-filtered transmission electron microscopy and X-ray reflection. The final layout appears to be strongly influenced by the structural features of the as-deposited multilayer. Threshold values of Si-rich carbide sublayer thickness and Si-to-C ratio are identified in order to preserve the ordered structure. The crystallized fraction is observed to be correlated with the total silicon volume fraction. The constraints are examined through the use of ab-initio calculations of matrix-embedded silicon nanocrystals, as well as in terms of existing models for nanocrystal formation, in order to establish the role played by the interface energy on nanocrystal outgrowth, residual amorphous fraction, and continuous crystallization. A parameter space of formation of ordered Si nanocrystals is proposed. The diffusivity of carbon in the crystallized material is evaluated, and estimated to be around  $10^{-16}$  cm<sup>2</sup>/s at 1100 °C.

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## 1. Introduction

Silicon nanocrystals (Si NCs) find their application in microelectronics and optics in devices such as discrete-trap storage nodes for fast-switching memories or optical waveguides [1]. The unique property of tuneable band gap [2], achieved through the control of NC diameter, is presently raising interest for application in photovoltaics as top absorber material in all-silicon tandem solar cells [3–6].

Size-controlled Si NCs embedded in a wide band gap matrix, typically SiO<sub>2</sub>, can be produced via the multilayer method, that consists in the deposition of alternate Si-rich oxide (SRO)/SiO<sub>2</sub> layers,

followed by solid phase crystallization. [2]. The method allows for an independent control of the Si grain size and density.

The efficient confinement associated to the wide band gap of SiO<sub>2</sub> brings about the drawback of poor electrical transport even under high electric field [7], which represents a limitation in electrical devices where efficient carrier transport is required. Efficient carrier transport is expected with a decrease of the band gap of the confining matrix, which has shifted the focus of investigation to a lower band gap material such as silicon carbide [8–15].

With respect to the SiO<sub>2</sub> matrix, the control of Si NC diameter in SiC is not straightforward. In the Si-rich carbide (SRC)/SiC system, the onset of Si crystallization varies between 800 °C and 1100 °C depending on the multilayer layout [9,10,14], with crystallized fraction and NC size increasing for higher temperatures [9,14]. The high thermal budget required to achieve effective crystallization causes the multilayer structure to vanish, and difficulties in confining the Si grain growth have been reported by several authors [9,10,12,14,16]. Considerable Si and C interlayer migration is observed for annealing temperatures higher than 1000 °C [10].

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The aim of this paper is to outline the processes occurring in the Si/SiC system, with the intent of identifying the mechanisms that govern the formation of Si NCs in SiC, impact on the final crystal size, and determine the persistence of the residual amorphous fraction. The survival of the multilayer, the bilayer thickness and the nanocrystal size will be determined by energy-filtered transmission electron microscopy (EF-TEM) and X-ray reflectivity (XRR). The crystalline degree will be evaluated by combining Raman scattering, X-ray diffraction (XRD) and UV–vis spectroscopy, and correlated with the multilayer parameters. A theoretical model based on the Density Functional Theory (DFT) will be applied to the Si NC/3C-SiC system, in order to determine the impact of lattice mismatch on nanoparticle structure, for varying nanoparticle sizes. The results will be discussed in terms of existing models for nanocrystal nucleation and growth, and will be put together to delineate a parameter space of formation of Si nanocrystals. The work is intended to contribute to the understanding of the SRC/SiC system and provide a key step forward regarding material engineering and design of devices.

## 2. Experimentals

SRC/SiC multilayers (=ML) were fabricated by PECVD on quartz and (100) CZ c-Si substrates. All layers were deposited in a plasma

of SiH<sub>4</sub>, H<sub>2</sub> and CH<sub>4</sub> at 13.56 MHz frequency and 28 mW/cm<sup>2</sup> power density. The SiH<sub>4</sub>/CH<sub>4</sub> gas flow ratio was varied in order to achieve the desired silicon rich carbide Si<sub>x</sub>C<sub>1-x</sub> composition. Details on deposition conditions are given in Table 1. The pressure of the gas mixture was adjusted in order to obtain ±5% homogeneity over the (8 × 8) cm<sup>2</sup> deposition clear area. The multilayers were composed of 30+31 layers, with SiC as the first and the last layer. The first deposited SiC layer was 20 nm thick, intended to prevent epitaxial regrowth driven by the c-Si substrate, as we have observed for lower buffer layer thickness in test samples (unpublished result). Several combinations of SRC composition and SRC and SiC as-deposited thickness ( $d_{\text{SRC}}^0$  and  $d_{\text{SiC}}^0$  respectively) were studied. The multilayers are grouped into four sets, labeled with a letter (X or D) followed by a number. The letter indicates the parameter that is kept constant in the SRC, either the Si ratio (X) or the thickness (D). The number stands for the as-deposited SiC thickness  $d_{\text{SiC}}^0$  expressed in nm. In particular:

Set X3	$x=0.95$	$d_{\text{SiC}}^0=3$ nm	$d_{\text{SRC}}^0=2,3,4$ nm
Set X9	$x=0.85$	$d_{\text{SiC}}^0=9$ nm	$d_{\text{SRC}}^0=2,3,4$ nm
Set D3	$d_{\text{SRC}}^0=3$ nm	$d_{\text{SiC}}^0=3$ nm	$x=0.6, 0.65, 0.75$
Set D5	$d_{\text{SRC}}^0=3$ nm	$d_{\text{SiC}}^0=5$ nm	$x=0.65, 0.75$

where  $d_{\text{SRC}}^0$  stands for the as-deposited value of SRC thickness.

**Table 1**

PECVD deposition conditions of Si<sub>x</sub>C<sub>1-x</sub> layers. Conditions common to all depositions: 13.56 MHz frequency, and 28 mW/cm<sup>2</sup> power density.

Sample set	Layer classification	Si ratio ( $x$ )	SiH <sub>4</sub> (sccm)	CH <sub>4</sub> (sccm)	H <sub>2</sub> (sccm)	$p$ (hPa)	$T_{\text{Substrate}}$ (°C)
X3	SRC	0.95	20	30	10	0.85	350
	SiC	0.5	1.6	70	0	0.9	350
X9	SRC	0.85	13	13	90	0.7	325
	SiC	0.5	2	70	100	0.9	325
D3	SRC	0.75	11.4	70	10	0.95	350
	SRC	0.65	6.1	70	10	0.95	350
	SRC	0.6	3	70	10	0.95	350
	SiC	0.5	1.6	70	10	0.95	350
D5-1	SRC	0.65	6.1	70	10	0.95	350
	SiC	0.5	1.6	70	10	0.95	350
D5-2	SRC	0.75	11.4	70	10	1	350
	SiC	0.5	2.6	70	10	1	350

**Table 2**

Multilayer parameters: silicon ratio  $x$ , as-deposited SiC and SRC thickness on quartz substrate; SiC, SRC, SiC+SRC bilayer thickness; nanocrystal size obtained by TEM and XRD.  $d_{\text{SRC+SiC}}$  was determined by TEM, or deduced from total thickness divided by the number of deposited double layers for non-surviving ML structure.  $d_{\text{SiC}}$  and  $d_{\text{SRC}}$  were determined as described in Section 2. Note that the statistical error on  $d_{\text{SRC+SiC}}$  is sometimes lower than the sum of errors on  $d_{\text{SiC}}$  and  $d_{\text{SRC}}$ .

Sample	$x$	Multilayer structure					Nanocrystal size	
		$d_{\text{SiC}}^0$ (nm)	$d_{\text{SRC}}^0$ (nm)	$d_{\text{SiC}}$ (nm)	$d_{\text{SRC}}$ (nm)	$d_{\text{SiC+SRC}}$ (nm)	TEM (on C–Si) (nm)	XRD (on quartz) (nm)
X3-1	0.95	3	1	1.8 ± 0.2	0.7 ± 0.5	2.5 ± 1.0 <sup>a</sup>	3 ± 2	
X3-2	0.95	3	2	1.8 ± 0.2	1.8 ± 0.2	3.5 ± 1.0 <sup>a</sup>	5 ± 2	
X3-3	0.95	3	3	1.8 ± 0.2	2.6 ± 0.2	4.5 ± 0.5	3.5 ± 1.5	
X3-4	0.95	3	4	1.8 ± 0.2	3.5 ± 0.2	5.4 ± 0.5	3.5 ± 2	
X9-2	0.85	6	2	5 ± 1	2 ± 0.5	6.7 ± 0.1 <sup>a</sup>		
X9-3	0.85	6	3	5 ± 1	3 ± 0.5	7.6 ± 0.1	4.7 ± 0.3	1.5 ± 1.0
X9-4	0.85	6	4	5 ± 1	4 ± 0.5	9.9 ± 0.5	5 ± 1	4 ± 0.5
D3-1	0.75	3	3	1.7 ± 0.5	2.0 ± 0.5	4.1 ± 0.1 <sup>a</sup>	5 ± 1	
D3-2	0.65	3	3	1.7 ± 0.5	2.0 ± 0.5	4.0 ± 0.1 <sup>a</sup>		
D3-3	0.6	3	3	1.7 ± 0.5	2.0 ± 0.5	4.1 ± 0.1 <sup>a</sup>		
D5-1	0.65	6	3	3 ± 1	2.5 ± 0.5	5.5 ± 0.5 <sup>a</sup>	5 ± 1	
D5-2	0.75	6	3	3 ± 0.5	3.5 ± 1.5	6.0 ± 0.2	4 ± 2	

<sup>a</sup> Deduced from total thickness divided by the number of deposited double layers.

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